

**LOW LOSS AND HIGH TOLERANCE OUT-OF-PLANE SINGLE-MODE  
OPTICAL INTERCONNECTIONS IN GLASS INTERPOSERS**

A Thesis  
Presented to  
The Academic Faculty

by

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In Partial Fulfillment  
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# **LOW LOSS AND HIGH TOLERANCE OUT-OF-PLANE SINGLE-MODE OPTICAL INTERCONNECTIONS IN GLASS INTERPOSERS**

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*Dedicated to my family.*

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## SUMMARY

The proliferation of mobile devices have resulted in an unprecedented increase in global data traffic. As the demand for bandwidth increases, electrical interconnects are limited by high frequency electromagnetic effects, making ways for optical interconnects to replace their electrical counterparts at shorter and shorter transmission distances. However, the migration to optical communication have been stalled by the high cost in fabrication and packaging of the many components required – optical fiber, laser, and photodetector to name a few. Unlike in telecommunication where the long transmission distance justifies expensive and bulky packaging, short-distance optical communication requires careful balance of cost, performance, and density of the package.

Silicon photonics and board-level optoelectronics have been intensely researched to enable short-distance optical communication. Silicon photonics promise the highest integration density by combining photonics and electronics on a single die using CMOS (Complementary Metal-Oxide Semiconductor) compatible processes. However, silicon photonics combines the two using the expensive Silicon-on-Insulator (SOI) technology, where the process requirements for the electrical layers are not compatible with that of the photonics layer. These issues limit silicon photonics to a chip-level technology needing a packaging solution. Board-level optoelectronics utilizes low cost substrate process technology to create optical Printed Circuit Boards (O-PCB) where all of the components can be assembled. However, O-PCB lacks the micron-level precision required to couple light to single-mode optical fibers, which means lower channel density plastic optical fibers are used. As a result, O-PCBs are only usable in low bandwidth applications.

In contrast to the prior approaches described above, the 3D glass photonics (3DGP) technology developed in this thesis is a lower cost alternative to silicon photonics and higher density choice to board-level optoelectronics at lowest power consumption. Optically, the refractive index of glass can match that of glass optical fibers to enable low loss light coupling. Electrically, the low loss tangent for glass is superior to silicon. Mechanically, the Coefficient of Thermal Expansion (CTE) of glass can be tailored to match that of either silicon or laser to improve the system-level reliability. Lastly, glass has the potential for low cost coming from large panel manufacturing utilizing lower cost package substrate processes.

The specific focus of this dissertation research is to design and demonstrate low loss and high tolerance out-of-plane single-mode fiber-to-chip optical interconnections in glass to address three challenges in performance, density, and cost: 1) high fiber-to-chip coupling loss, 2) lack of high density fiber-to-chip coupling solutions, and 3) high cost active fiber alignment. Four research tasks are defined, one task each to address each challenge, and a fourth task focused on a demonstration test vehicle. The optimized optical interconnection is able to achieve  $< 2$  dB of coupling loss at fiber-like alignment tolerance. It includes a parallel-processed  $45^\circ$  turning mirror using moving mask lithography. The novel moving mask process ensures that the turning mirror and the pads for chip assembly are planar aligned with only micron level offset. In addition, fiber alignment u-grooves are fabricated in glass with aims to allow passive fiber assembly. Although the research results did not meet the passive alignment criterion, future direction has been defined based on these results.

A co-design process flow has been developed to optimize the demonstration test vehicle, which emulates a 400 Gbps optical transceiver module. The test vehicle features optimized electrical

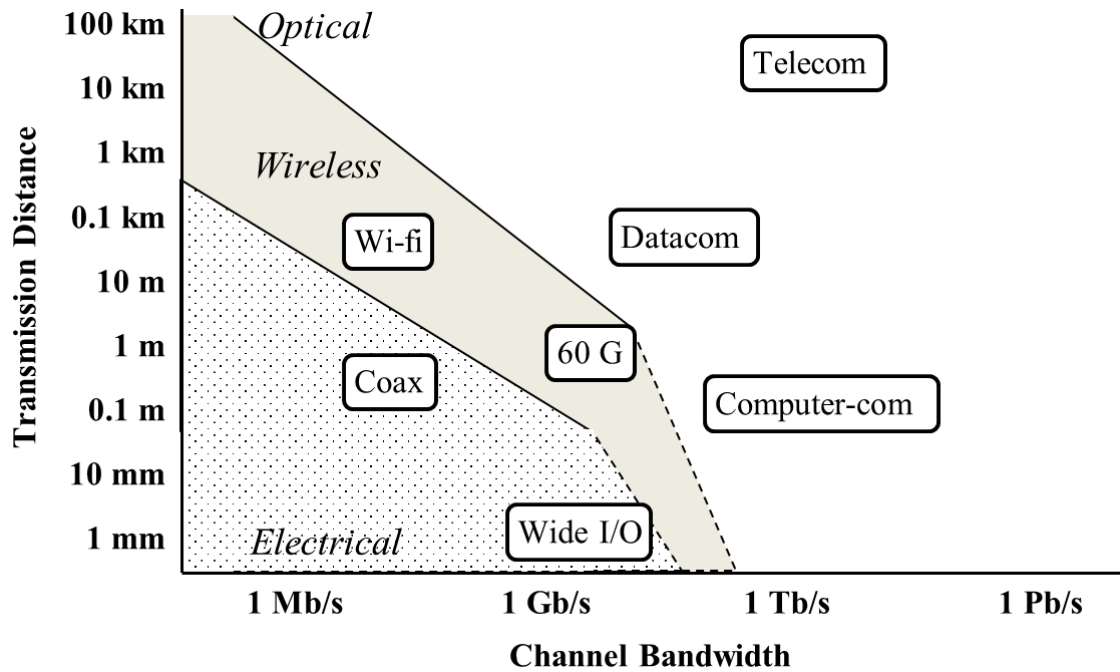
interconnects at  $< 0.1$  dB/mm insertion loss, thermal vias to keep laser temperature under  $80\text{ }^{\circ}\text{C}$ , as well as the low loss and high tolerance out-of-plane optical interconnections as discussed. The results demonstrate compelling evidences in the cost, performance, and density advantages of glass interposer technology for photonics applications.

# CHAPTER 1

## INTRODUCTION

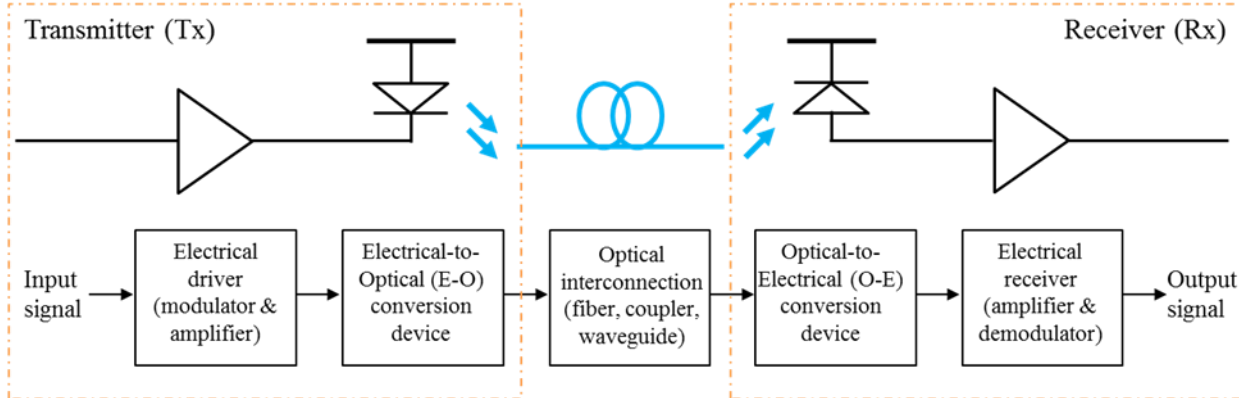
Mobile devices such as smartphones and wearables, as well as the move to cloud-based data storage, have resulted in an unprecedented increase in global data traffic, which is projected to double to over 180 Exabytes ( $10^{18}$  bytes) per month from 2016 to 2019 [1]. This demand for bandwidth has transformed the electronic industry from computing driven, as dictated by Moore's law, to communication driven, as dictated by data rate. As a result, the bottleneck for the next generation of electronics is in system level scaling of interconnects, rather than chip level transistor scaling [2].

The three main methods for data transmission, namely, wired (electrical), wireless, and optical are plotted as a "bandwidth-distance" relationship as shown in Figure 1.1 [3], [4]. Optical communication has been the dominant method for data transmission in the telecommunication industry due to the unmatched propagation loss ( $>0.25$  dB/km) and channel bandwidth ( $>1$  Tb/s/ch by wavelength division multiplexing) of optical fibers [5]. However, the inherent high cost in the fabrication and assembly of optical communication systems have limited them to long distance where the propagation loss of electrical wiring is simply unacceptable. As the demand for channel bandwidth continues to increase, electrical communications are limited by high frequency electromagnetic effects such as propagation delay, signal-to-signal crosstalk, and reflection. Optical communications, being relatively immune to these effects, have become more attractive in shorter distances [6]. As shown in the figure, optical interconnections are expected to reach board-board (Computer-com, or High Performance Computing) level, where the per-channel bandwidth requirement is close to 1 Tb/s/ch at distances below 30 centimeters (1 foot).



**Figure 1.1. The divide between optical, wireless, and wired electrical communication technologies based on transmission distance versus bandwidth (bandwidth-distance)**

For optical communications to be used at board-board level, cost and power consumption must come down significantly. To understand the enablers for further scaling of optical communications, one must first look at a basic optical communication system. An optical communication system of any length can be broken into a transmitter (Tx) and a receiver (Rx) package, with **optoelectronics devices**, **optical interconnection**, and **electrical interfaces**, as shown in Figure 1.2. The optoelectronics devices convert the signal between electrical and optical domains by a laser (E-O) or a photodiode (O-E). The optical interconnection consists of optical waveguides, fibers, and coupling structures in between the optoelectronics devices. The electrical interface serves mainly to amplify the electrical signal as it is transmitted from or received into the computing unit, respectively. As transmission distance shrinks, the high bandwidth and low loss advantages of the optical fibers are no longer compelling enough, because the optoelectronics packages do not shrink with distance.



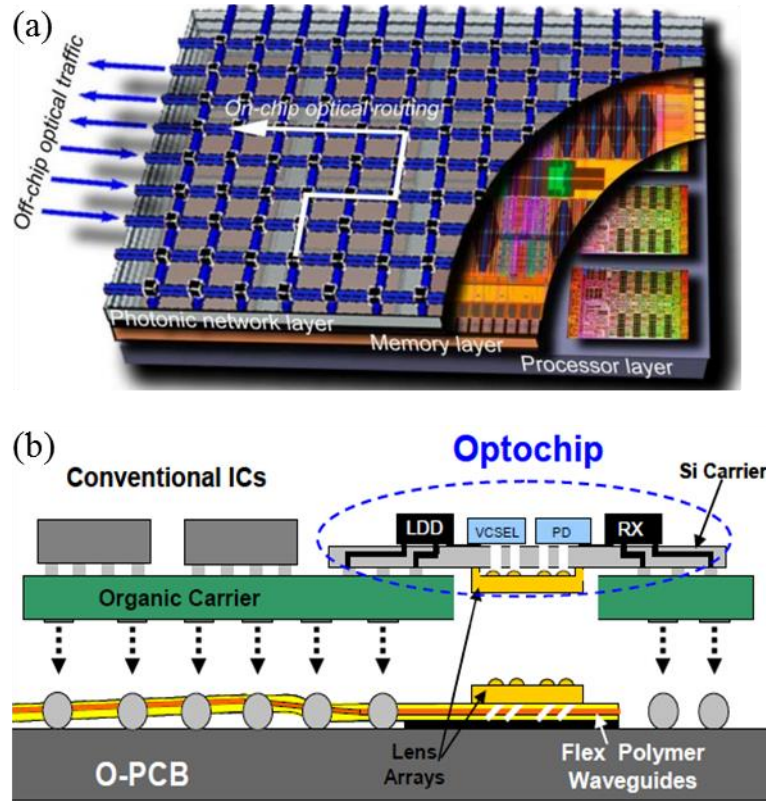
**Figure 1.2. Anatomy of a typical optoelectronics communication system**

### 1.1 Current Approaches to Optoelectronics Packaging

Current approaches to optoelectronics packaging have focused on optimizing the cost, power, and density at system level [4]:

- **Cost:** The cost is comprised of chip fabrication, substrate fabrication, assembly, test, and yield. Due to the tight tolerance requirements, the optical fiber and chip assembly make up approximately 50 % of the overall cost [7].
- **Power:** The power budget consists of chip power consumption, chip-to-fiber coupling loss, and the electrical transmission loss of the driver circuitry. The power is expressed as “energy efficiency” in Joules per bit (J/b) [8].
- **Density:** The package size must decrease to minimize fiber-to-chip distance, with higher bandwidth per channel as dictated by the bandwidth-distance relationship. The density is expressed as bitrate per package area (Tbps/cm<sup>2</sup>).

Two current optoelectronics packaging approaches, shown in Figure 1.3, have been intensely researched to address the above needs: **silicon photonics** and **board-level optoelectronics**.



**Figure 1.3. Board-board optical communication system by (a) silicon photonics and (b) board-level optoelectronics [9], [10]**

### 1.1.1 Silicon Photonics

Similar to System-on-Chip (SoC) technology, silicon photonics focuses on on-chip integration by combining photonics and electronics on a single die using CMOS (Complementary Metal-Oxide Semiconductor) compatible processes. Pioneering research done at Intel and IBM have shown the promise of silicon photonics to reach high density at  $> 30 \text{ Tbps/cm}^2$  and high energy efficiency of  $< 1 \text{ pJ/b}$  [11]. However, the lack of direct bandgap in silicon means III-V semiconductor compound lasers need to be integrated separately, thus making true “monolithic” integration not practical. More importantly, silicon photonics is built using Silicon-on-Insulator (SOI) technology, which requires an expensive buried oxide (BOX) layer, thus making chip cost

a major concern. Lastly, just as digital and analog integration is a challenge in SoC, the process requirements for photonic circuitry ( $> 300$  nm in line width) are not compatible with those for digital circuitry (10 nm gate length). These issues limit silicon photonics to a sub-system level solution, with challenges in addressing the cost requirements of a short distance optical transmission system.

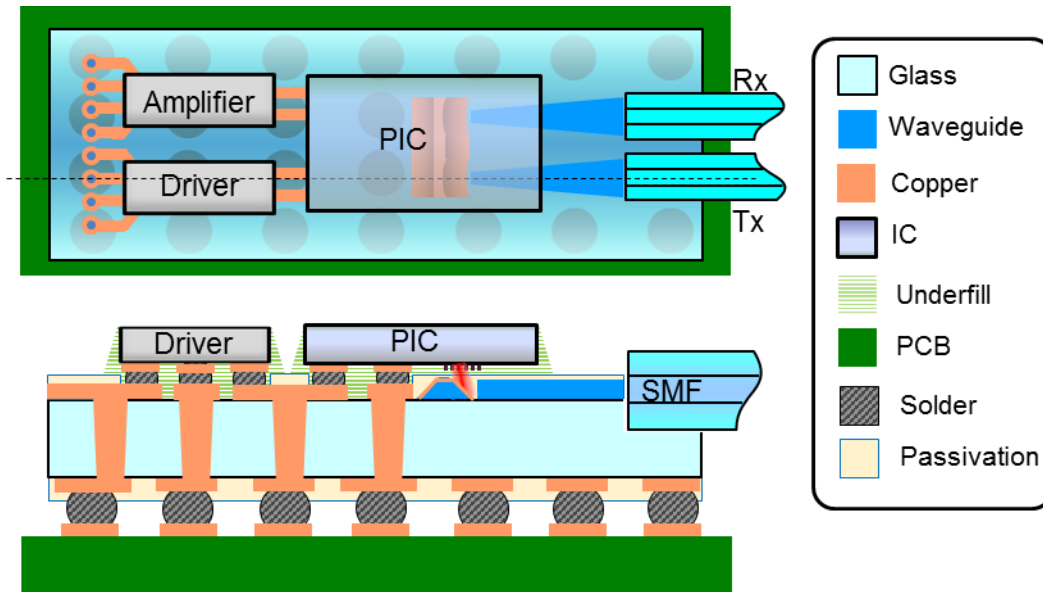
### **1.1.2 Board-Level Optoelectronics**

Traditionally, optoelectronics devices and fibers have been assembled on an expensive substrate called “silicon optical bench” (SiOB). SiOB has since been replaced by silicon interposer, where high cost fiber alignment structures can be moved to board level [12]. IBM research has demonstrated this concept in its Terabus research program [10]. However, the Coefficient of Thermal Expansion (CTE) mismatch between silicon and Printed Circuit Board (PCB) necessitates a buffering “organic carrier” layer, to ensure the reliability of interposer, thus complicating the system. Further, the high speed electrical loss of silicon degrades the energy efficiency of silicon interposers. Finally, silicon interposers made with CMOS technology are still expensive compared to organic substrates. While capable of a small reduction in cost at the expense of system power and density, silicon interposers may not be the best packaging technology for long term scaling of optical interconnections for cost, power and size.

## **1.2 Unique Approach – Optoelectronics with Glass Interposer**

Glass interposers, pioneered at GT-PRC, have emerged in recent years as a superior option to silicon and organic interposers for mobile and 2.5 D applications [13], [14]. This thesis proposes a unique packaging approach based on 2.5D and 3D glass photonic interposers as shown in Figure 1.4.





**Figure 1.4. Glass-based optoelectronics packaging proposed in this thesis**

Glass offers a unique combination of optical, electrical, and thermo-mechanical properties, and large area processability, unmatched by other materials. Optically, the refractive index of glass can match that of glass optical fibers. In addition, the optical transparency of glass can be utilized to fabricate optical circuitry without the expensive BOX layer required for silicon photonics. Electrically, the low loss tangent for glass is far superior to silicon, and the lower dielectric constant also enables higher data rates. Mechanically, the CTE of glass can be tailored to match the CTE of either a silicon Photonic Integrated Circuit (PIC) or a III-V compound semiconductor laser, thus improving the system-level reliability. The CTE matching also enables precision assembly of photonic ICs, crucial for low loss optical coupling not possible in organic materials. The low surface roughness and high dimensional stability glass can achieve  $1\mu\text{m}$  features similar to silicon processes not possible in organic materials, for higher interconnect density and precise coupling to optical fibers. Lastly, glass has the potential for low cost coming from large panel manufacturing

utilizing lower cost package substrate processes not possible in silicon materials. Table 1.1 compares glass and silicon against the key metrics for optoelectronics packaging.

**Table 1.1 Comparison of materials for photonics interposer application**

Material Properties		Glass	Silicon	Organic
Optical absorption, $\alpha$ [ $\text{cm}^{-1}$ ]	850 nm	0.002	760	N/A
	1550 nm	0.007	8.2	N/A
Refractive index, $n$ , @ 1550 nm		1.49	3.48	N/A
Electrical loss, $\tan \delta$ @ 10 GHz		0.006	0.015	0.009
CTE (ppm/K)		3 – 8.5	3	17
Surface roughness, $R_a$ [nm]		< 1	0.15 – 0.3	300 – 580
Finest feature size [ $\mu\text{m}$ ]		1 - 10	0.1 – 1	> 10
Process technology		Panel	Wafer	Panel

Due to the limited use of glass as an interposer material, optical interconnection technologies in glass have yet been fully explored. Initial research done by Fraunhofer Institute has demonstrated an optical transceiver module using the glass substrate as a waveguide [15]. However, the optical confinement of such waveguides is very weak, rendering them impractical for high density and high performance optical interconnection, where stronger light confinement is required. Further, the amorphous nature of glass does not lend itself to precise micro-structuring of fiber alignment grooves, making fiber assembly a challenge. The research to be presented in this thesis identifies these challenges and aims to address them by unique approaches in glass.

### 1.3 Research Objectives and Technical Challenges

The objective of this research is to design and demonstrate a low loss and high tolerance out-of-plane single-mode fiber-to-chip optical interconnections in ultra-thin glass interposers to meet the power, density, and cost requirements for short distance optical communication systems. This research focuses on fundamental understanding of each component of the out-of-plane fiber-to-chip coupling structure by optical modeling, design, fabrication, and characterization.

The research can be broken down into three succinct research objectives as summarized in Table 1.2. The table also identifies the state-of-art research results reported for each objective, the associated technical challenges that need to be addressed, and the specific research task proposed in this thesis to address each challenge. Each research objective and its associated challenges is discussed in more detail next.

**Table 1.2. Research objectives, SOAs, challenges, and tasks to address them**

<b>Objectives</b>	<b>State-of-art (SOA)</b>	<b>Challenges</b>	<b>Research Tasks</b>
Low loss optical interconnections	2 dB VGC-to-fiber coupling loss [16], [17]	High mode mismatch loss	Large core optical waveguides and vias in glass
Out-of-plane turning at low cost	Angle polished fiber to VGC or WG [18], [19]	High density chip-to-fiber integration	Planar processed turning mirrors by moving mask lithography
High tolerance fiber-to-chip alignment	$\pm 2 \mu\text{m}$ or $\pm 0.5^\circ$ fiber alignment tolerance to WG on silicon chip [20]	High cost active fiber assembly	U-groove in glass for passive alignment, optimize alignment tolerance

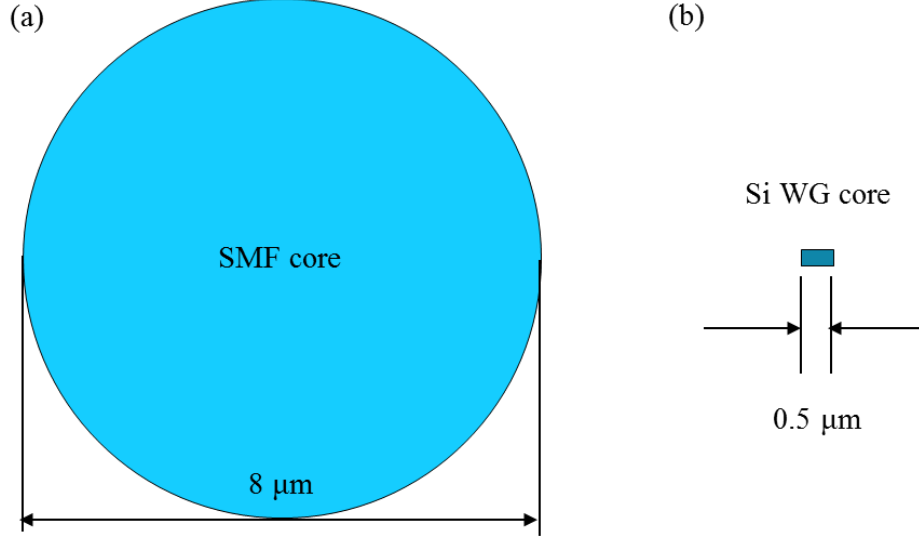
### 1.3.1 Low Loss Optical Interconnections

The optical interconnections are the interface between the optical fiber and the waveguide in an optoelectronic chip. Both the optical fiber and the waveguide operate by total internal reflection (TIR), where a core of higher index,  $n_c$ , is surrounded by a cladding layer with a lower refractive index,  $n_{cl}$ , thus the light remains confined at a constant reflection angle as it travels along the core. The guided light may be single-mode (SM) or multimode (MM) depending on how many reflection angle is allowed to propagate inside the core, with SM only allowing one such angle. Single-mode optics exhibit low modal dispersion, which enables effective implementation of channels with extremely high capacity ( $> 1$  Tb/s/ch) using techniques such as wavelength division multiplexing (WDM). As a result, single-mode optics have dominated high bandwidth research at short distances. In this thesis, only single-mode integration is considered.

Of crucial importance to the optical loss is the difference in size between the fiber and the waveguide on chip. The size of fiber/waveguide core is a function of the difference in refractive indices between core and cladding ( $\Delta n$ ) defined as:

$$\Delta n = \frac{n_c - n_{cl}}{n_{cl}}. \quad (1.1)$$

The core diameter of a single-mode fiber (SMF) is roughly  $8 \mu\text{m}$ , and it is one of the largest because the refractive index difference is only 0.4 % [21]. On the other hand, the refractive index difference of a silicon waveguide ( $n_c = 3.5$ ) on silicon dioxide ( $n_{cl} = 1.5$ ) is 57.1%. As the result, the typical core size of a silicon waveguide is  $0.5 \mu\text{m}$  by  $0.25 \mu\text{m}$ . A to-scale comparison of the fiber core and silicon waveguide core is shown in Figure 1.5.



**Figure 1.5. (a) The cross-section of the core of a single-mode fiber and a (b) silicon waveguide on chip**

The coupling loss between two single-mode guides can be approximated by Gaussian Beam Analysis. The simplified loss expression, assuming the two guides are lined up perfectly, is as follows:

$$\text{Coupling loss (dB)} = 10 \log\left(\frac{4A_1A_2}{(A_1 + A_2)^2}\right) \quad (1.2)$$

Where  $A_1$  and  $A_2$  are the cross-sectional areas of the two cores. In the case of fiber directly to silicon waveguide,  $A_1$  is  $16\pi \approx 50 \text{ μm}^2$ , and  $A_2$  is  $0.125 \text{ μm}^2$ . The resulting coupling loss is 20 dB, which means 99% of light is lost. This is a well-known challenge, and there are two popular solutions: a spot-size converter in-plane with the waveguide or a vertical grating coupler (VGC) converting the light-wave to out-of-plane operation. 2 dB of loss can be achieved by an optimized spot-size converter or a VGC [16], [17]. However, both solutions suffer a degradation in terms of integration density, which is discussed next.

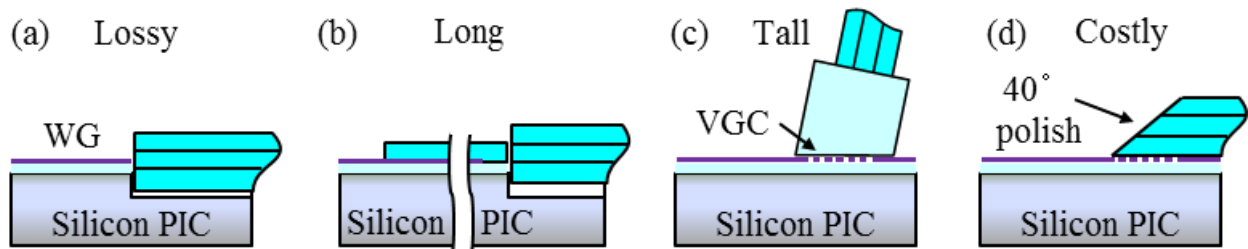
### 1.3.2 High Density Chip-to-Fiber Integration

The highest density integration is achieved if fiber can be directly assembled on chip either in-plane with direct fiber-to-waveguide coupling [18], or out-of-plane using grating couplers [19].

The in-plane solution has a high coupling loss and a very tight fiber-to-waveguide alignment tolerance. The spot-size converters mentioned in the previous section can address both problems, but spot-size converters have to be designed long enough to allow mode conversion, usually several millimeters thus adding to expensive chip area.

The out-of-plane assembly uses an angle-polished fiber block, polished at a slight angle for maximum coupling to VGC. However, the bending radius of the out-of-plane fiber block adds centimeters to the thickness of the package. In addition, this block must be active aligned since multiple degrees of freedom need to be controlled. To address the large package size, the use of a 40° polished fiber has been reported to allow planar fiber integration [22]. Although high integration density is achieved, active alignment is still needed. In addition, no high volume manufacturing solution for 40° polished fiber exist today, further making cost a challenge.

The four integration schemes described above are illustrated in Figure 1.6.

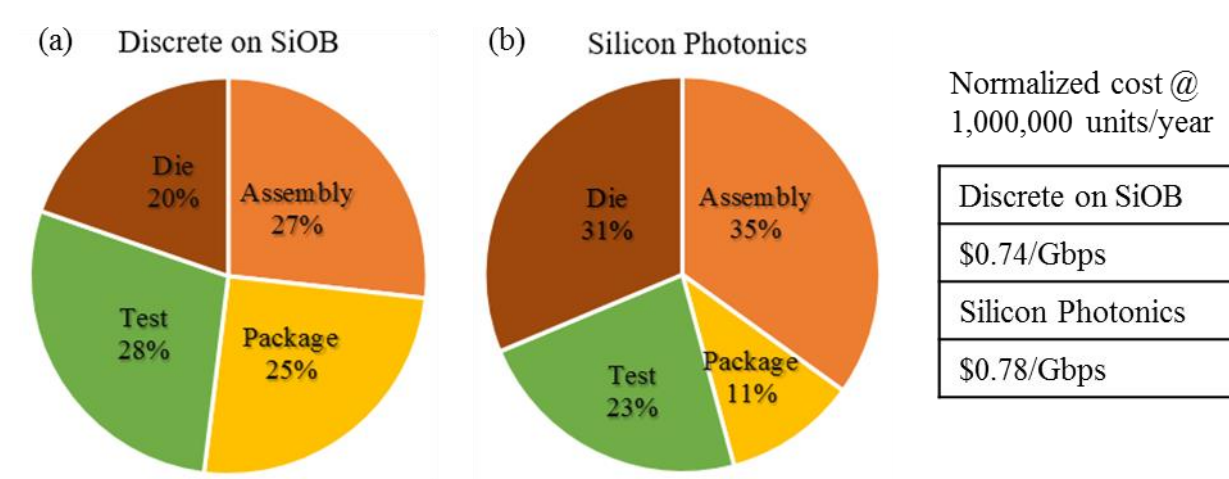


**Figure 1.6. Chip-to-fiber integration by (a) direct in-plane coupling, (b) in-plane spot-size converter, (c) out-of-plane fiber block, and (d) out-of-plane angle-polished fiber aligned with chip**

### 1.3.3 High Tolerance Fiber-to-Chip Alignment

Although the first two objectives can be achieved by some of the solutions thus described, none of them is low cost. Process Based Cost Modeling (PBCM), developed by the researchers at MIT, provided an insightful breakdown of overall manufacturing cost of a 100 Gbps optical transceiver package. Two integration schemes are compared: discrete chips on a silicon optical bench and monolithic silicon photonic integration. In both cases, active-aligned fiber directly coupled to in-plane waveguides is assumed. The estimated cost for 1,000,000 units per year is reproduced in Figure 1.7.

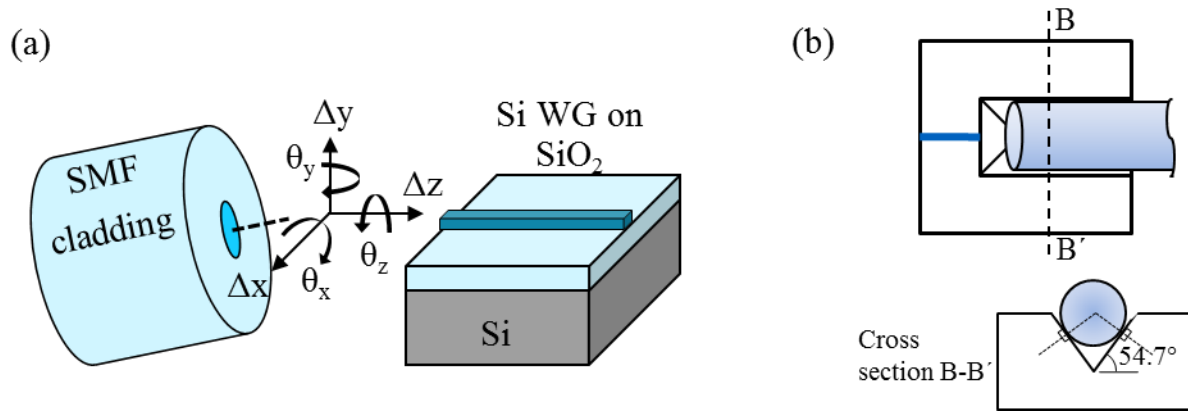
As seen from the figure, more than 50% of the cost is estimated to be from assembly and test. In fact, more than 75% of assembly and test cost involves the high precision active alignment and package-level testing needed to establish low loss chip-to-fiber interconnection. This highlights the importance to design for high tolerance assembly to allow passive alignment and design for high tolerance fabrication to simplify testing at package level.



**Figure 1.7. Process based cost modeling of optical transceiver packages assuming 1,000,000 units per year using (a) heterogeneous and (b) monolithic integration**

Fiber assembly poses a major challenge due to the need to control six degrees of freedom ( $\Delta x$ ,  $\Delta y$ ,  $\Delta z$ ,  $\theta_x$ ,  $\theta_y$ ,  $\theta_z$ ). Gaussian Beam Analysis (more detail in Chapter 3) shows that, for direct fiber to silicon waveguide coupling, a 1  $\mu\text{m}$  or  $1^\circ$  misalignment in either  $\Delta x$ ,  $\Delta y$ ,  $\theta_x$ , or  $\theta_y$  is enough to introduce 3 dB of loss. The high cost active alignment process, which involved a laser-assisted scan of fiber with respect to the chip, is commonly used to achieve this level of precision. Passive alignment is the low cost alternative, which forgoes the laser scanning process by micro-machining of precise features on the substrate to limit the degrees of freedom. Silicon “v-groove,” for example, can constrain four degrees of freedom ( $\Delta x$ ,  $\Delta y$ ,  $\theta_x$ ,  $\theta_y$ ). By employing v-grooves, low cost pick-and-place assembly of fiber is possible as demonstrated by IBM [20]. However, the solution proposed by IBM requires custom tooling and uses an evanescent mode spot-size converter on chip, which requires high precision; therefore, the low cost assembly benefit is outweighed by low density integration and high cost fabrication.

Figure 1.8 illustrates the six degrees of freedom and the use of v-groove to help fiber integration.

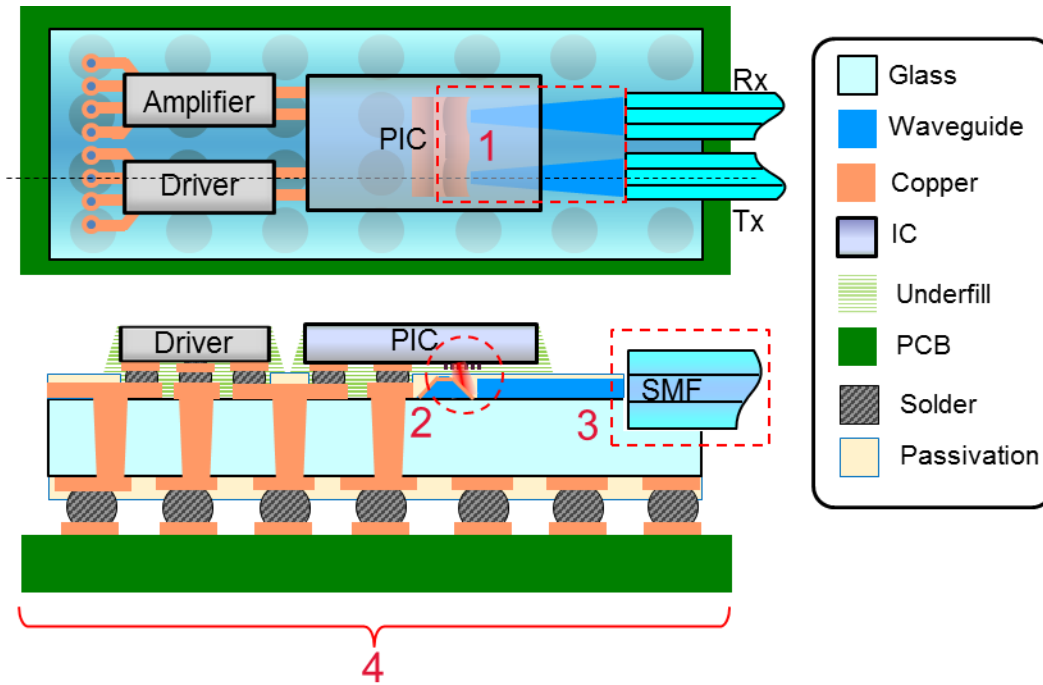


**Figure 1.8.** (a) Fiber-to-chip alignment is a challenge with six degrees of freedom, but (b) silicon v-grooves have proven to mitigate some of the variables



## 1.4 Research Tasks

Three research tasks have been identified to address the technical challenges associated with each research objective, with the additional task to build a demonstrator, as shown in Figure 1.9.



**Figure 1.9. The four research tasks to address the research challenges**

**Task 1:** To model, design, fabricate, and characterize low loss and high tolerance optical waveguides in glass. Mode-matched large core optical waveguide on glass can **minimize coupling loss** and **maximize alignment tolerance** to fiber. Both horizontal waveguides on the surface of glass and vertical waveguides through glass will be researched and investigated here.

**Task 2:** To model, design, fabricate, and characterize a novel planar processed out-of-plane turning mirror using moving mask lithography, and integrate the mirror with optical

waveguides from Task 1. This turning structure allows **low cost** and **high density** integration of photonic integrated circuit (PIC) on glass.

**Task 3:** To design and demonstrate precise optical fiber alignment structures fabricated directly in glass, with **high tolerance** interface to optical waveguides to enable passive fiber alignment. Specifically, u-groove structures fabricated directly on glass will allow **low cost** passive alignment of optical fibers to polymer waveguides on glass.

**Task 4:** To design and demonstrate an integrated test vehicle, with optoelectronic or electronic devices assembled, combining not just the optical interconnects, but electrical and thermal as well.

## 1.5 Dissertation Overview

The dissertation is organized as follows. This chapter provides the strategic need for the research topic, defines the research objectives, identifies and briefly describes the three main challenges to achieve the objectives, and outlines the unique approach and the research tasks to address the challenges. Chapter 2 summarizes the prior arts by first looking at system level research from silicon photonics perspective as well as from the SOP perspective, then focuses in on state-of-the-art research in optical interconnections. Chapter 3 describes in detail research task 1, the modeling, design, and fabrication of both horizontal and vertical optical waveguides for low loss and high tolerance in glass interposer. Chapter 4 discusses in detail research task 2, the modeling and process development of out-of-plane turning mirror using moving mask lithography. In addition, it discusses current work done to address task 3 in the design of u-groove alignment

structure. Chapter 5 describes tasks 4, the design and demonstration of integrated test vehicles combining the optical, electrical, and thermal interconnects, and the assembly of active devices. Chapter 6 provides a conclusion and discusses future work in the field beyond the scope of the dissertation.

## CHAPTER 2

### LITERATURE REVIEW

This chapter describes the prior work in four areas. The first section discussed the prior art in optical interconnections at system level, focusing on multimode and single-mode research in board-board optical communication systems. The following sections cover the published literature by other researchers in addressing the technical challenges defined in Chapter 1.

#### 2.1 System-Level Board-Board Optical Interconnections

This section describes selected published literature in the area of optical interconnections at system level and is organized into multimode and single-mode approaches to optical communications.

##### 2.1.1 Multimode Approach to Optical Communications

The multimode approach to short distance optical communication evolves directly from Datacom systems consisting of 1D or 2D VCSEL/PD arrays. The optical interconnections on these works consist of multimode waveguides, turning mirrors, and micro-lens arrays.

IBM's Terabus program is the most prominent example of such systems, with a reported terabit/sec-class bandwidth [10]. The stack-up, shown in Figure 2.1, consists of the silicon interposer on top of an organic carrier. An organic carrier is needed to resolve the CTE mismatch between the silicon interposer and the organic substrate. The multimode optics include an out-of-plane turning mirror built in the embedded polymer waveguides located on the organic substrate. Dual micro-lens arrays are assembled on the bottom of the silicon interposer and on top of the organic substrate to improve the alignment tolerance between the interposer and the substrate to  $> 20\text{ }\mu\text{m}$ . However, the lens must also be aligned to the optical vias in silicon interposer, with  $< 5$

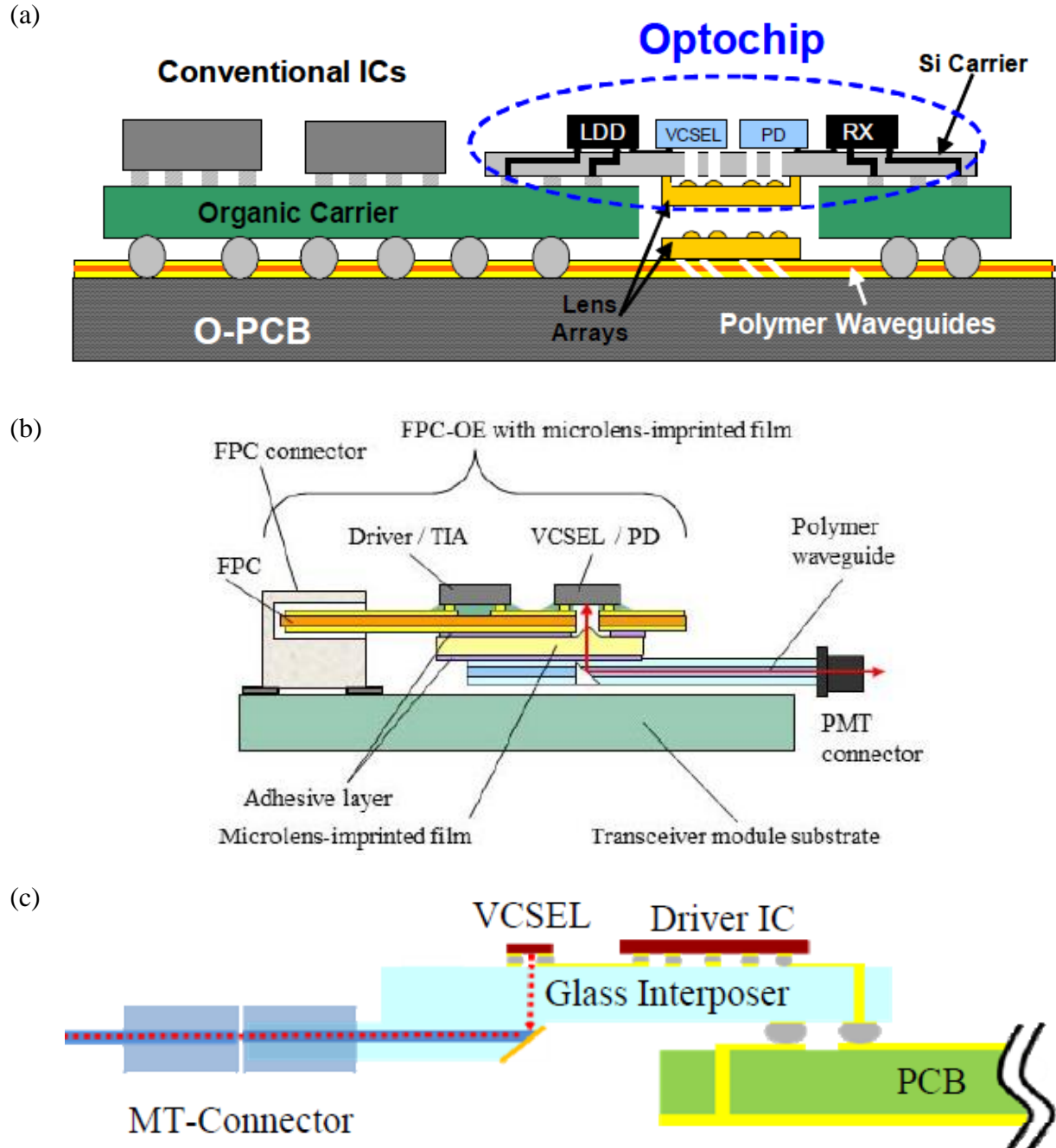
$\mu\text{m}$  tolerance. Optical “holey vias” are etched in silicon interposer to allow light to pass, as silicon is not transparent at 850 nm. Fiber coupling is achieved by MT ferrules on organic substrate.

Similar research works based on VCSEL arrays have been demonstrated on organic interposers by Georgia Tech, NGK/NTK, and Fujitsu [23], [24], [25]. Although lower cost and less complex than a silicon interposer, the inferior dimensional stability of organic interposers limit VCSEL/PD to 1D arrays, thus terabit bandwidth is not achievable.

Fraunhofer IZM’s EOCB (Electro-Optical Circuit Board) program is the first to promote glass interposers and first to use glass itself as gradient multimode optical waveguides [15]. While the optical loss achieved is impressive ( $< 0.15$  dB/cm at 850 nm), the complicated silver ion-exchange process can only achieve weakly confined waveguides that are incapable of performing high density routing.

The Terabus program, and all the other research programs based on multimode optics, were inherently limited by channel bandwidth. With amplitude modulation such as on-off-keying (OOK) as the only modulation scheme suitable for VCSELs, the channel bandwidth was typically no more than 28 Gbps, with 56 Gbps demonstrated in ideal lab environment [26].

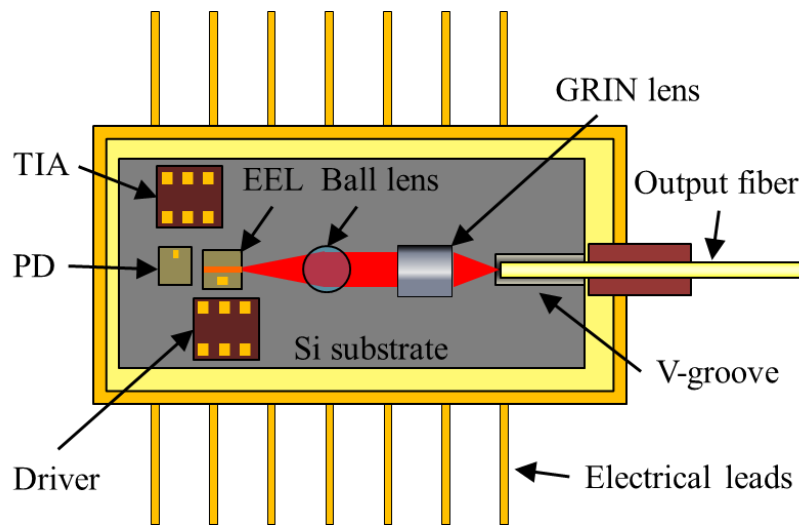
Despite the impressive research results, the complex integration and the limited channel bandwidth have made commercialization of board-board multimode systems impractical irrespective to interposer technology. As a result, most of these research programs have been either terminated, as in Terabus, or have shifted the focus to Active Optical Cables for Datacom, as in NGK/NTK and Fujitsu. A side-by-side comparison of IBM, Fujitsu, and Fraunhofer IZM’s approaches is shown in Figure 2.1.



**Figure 2.1.** The multimode approach to short distance optical communication. Prior works have demonstrated (a) silicon interposer, (b) organic interposer, and (c) glass interposer integration [10], [15], [25]

### 2.1.2 Single-mode Approach to Optical Communications

Single-mode optics can achieve orders of magnitude higher channel capacity (500 Gbps vs 25 Gbps) by wavelength division multiplexing (WDM) which is impractical to implement in multimode optics due to intermodal dispersion. Traditionally, single-mode optics have been implemented as discrete components on a silicon optical bench (SiOB), as shown in Figure 2.2. SiOB relies on precise etching of alignment structures on silicon to allow passive alignment [27]. While SiOB offered a reliable substrate, the many discrete components required – ball lens, lasers, photo-detectors, modulators, and amplifiers, to name a few – complicate assembly and require a large substrate area to integrate. As a result, SiOB has been used primarily for telecommunication systems where performance trumps concerns for density and cost.



**Figure 2.2. Discrete integration of single-mode optics based on Silicon Optical Bench**

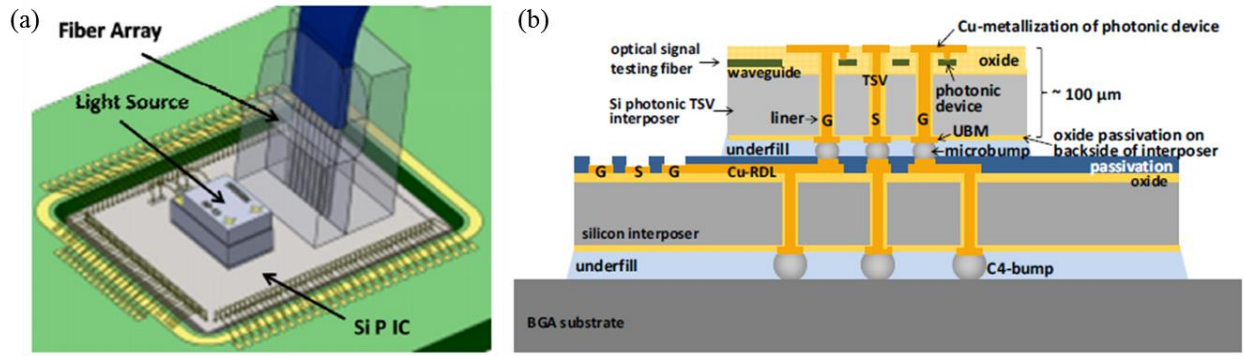
Silicon photonics technology is an evolution of SiOB that offers highest integration density, with WDM based optical transceiver chips already in the market [28]. However, as mentioned in Chapter 1, high chip cost have kept silicon photonics to limited used in high end

telecommunications or high performance computing research [29], [30]. Recently, silicon photonics have gained momentum in short distances communications for several reasons. First, with the increased bandwidth demands beyond 50 Gbps per channel, electrical interconnections and multimode optical interconnections cannot compete in energy efficiency [31]. In addition, silicon photonics design kits and fabrication foundries have finally become affordable after years of development, for example the ePIXfab in Europe. As a result, many companies are now aggressively pursuing single-mode optical transceivers based on silicon photonics technology: Luxtera, Finisar, Cisco, and Intel, to name a few.

Luxtera has been the pioneer in silicon photonics packaging, having demonstrated a silicon photonics chip with assembled laser dies and vertical integration of optical fiber array housed in an organic substrate [32]. The fiber integration scheme, first developed by CEA-LETI (Laboratoire d'électronique des technologies de l'information), can achieve low loss fiber coupling by active alignment process [33]. In the above approaches, the silicon photonics chip is wire-bonded to organic substrate, which is a concern for both high speed and high density electrical transmission. To address this, flip-chip based silicon photonics dies assembled on “silicon photonics interposers” have recently been proposed and demonstrated by the A\*STAR (Agency for Science, Technology, Technology, and Research) team from Singapore [34]. The introduction of silicon photonics interposer to perform both electrical redistribution and optical coupling can improve integration density while reducing die cost. However, it remains to be seen if silicon photonics interposer will ever be a low cost solution. The results from Luxtera and A\*STAR are reproduced in Figure 2.3.

On the other hand, Finisar has been developing a low-cost glass interposer solution for both optical and electrical interconnections [35]. No published results are available from Finisar at the writing of this thesis. It remains to be seen whether their solution can achieve manufacturability.





**Figure 2.3. (a) Luxtera's silicon photonics packaging solution featuring vertically assembled fiber array and (b) A\*STAR's silicon interposer approach aimed at improving interconnection density [32], [34]**

Amongst all of the single-mode technologies listed above, the common challenge to be addressed is fiber-to-chip optical interconnections, which is reviewed next.

### 2.1.3 Fiber-to-Chip Optical Interconnections

Four types of coupling are possible between the photonics chip and the optical fiber. They are the permutation of two emission or detection directions, namely edge emitting or surface emitting, of the photonics chip, and the two fiber orientations with respect to said chip, namely in-plane or out-of-plane. In-plane coupling has been simpler to implement than out-of-plane irrespective to emission direction because fiber axis can be directly aligned to the propagation direction of the light, using the interposer or the device itself as reference point.

In the case of in-plane coupling to surface emitting chip, such as the approach used by Luxtera, fiber is directly coupled to a vertical grating coupler [33]. The coupling loss can be minimized to only the loss of grating coupler itself, provided that the mode field between the fiber and the VGC could be matched. However, since the emission is vertical to the surface of the interposer, the assembled fiber added a significant amount of height to the package.

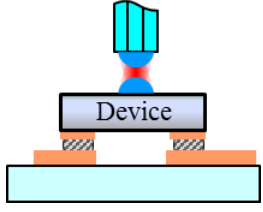
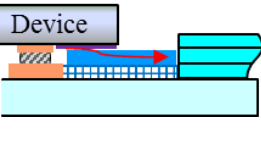
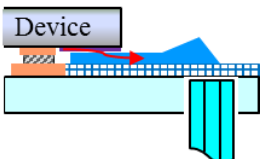
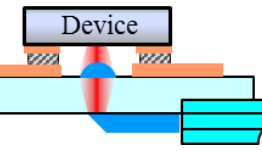
In-plane coupling to edge emitting chips, on the other hand, offered a compact form factor as well as low coupling loss using tapered waveguide couplers. All of the research on in-plane waveguide couplers are aimed at converting the spot size from that of a single-mode fiber to that of a silicon waveguide. One design utilizes a compact double stage tapered waveguides on chip with a recently reported loss of 1.5 dB [16], another design utilizes polymer to silicon waveguide adiabatic coupler showed a loss of 1 dB with  $\pm 2 \mu\text{m}$  tolerance [36]. The second design is able to achieve low loss by assembling the optoelectronic device directly on top of the polymer waveguides on substrate, making contact in due process. This method is further developed by IBM in their “silicon Nano-photonics” research, where edge coupling of waveguides to 1x12 single-mode fiber ribbon at 0.7 dB loss has been demonstrated [20].

There have been few research works on out-of-plane coupling to edge-emitting chips. The big reason is that the fiber will be vertical to the surface of the interposer, which, as in the in-plane surface emitting case, adds undesirable height. One such work demonstrated a novel J-coupler turning structure and a TSV for fiber integration with 16 dB of loss reported [37].

Out-of-plane coupling to surface emitting chips have not seen much research in single-mode integration due to the dominance of edge emitting chips. The emergence of vertical grating couplers (VGC) have provided high testability will likely shift that dominance. Initial works in this configuration have shown relative low coupling loss with high alignment tolerance and excellent density [22]. This thesis attempts to add to that knowledge. Three challenges have been identified with this approach: low loss planar waveguide for optical routing, out-of-plane turning, and planar fiber alignment. They are discussed next.

A quick comparison of the four types of device-to-fiber coupling is shown in Table 2.1.

**Table 2.1. Comparison of four types of fiber-to-chip optical interconnections**

Configuration	In-plane, surface emitting	In-plane, edge emitting	Out-of-plane, edge emitting	Out-of-plane, surface emitting
Structure				
Coupling loss	1.5 dB	0.7 dB	16 dB	1.6 dB
1 dB tolerance	$\pm 2.5 \mu\text{m}$	$\pm 2 \mu\text{m}$	N/A	$\pm 2.6 \mu\text{m}$
Height	> 5 cm	< 1 mm	> 5 cm	< 1 mm
Testability	High	Low	Low	High

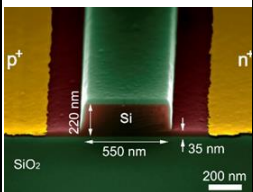
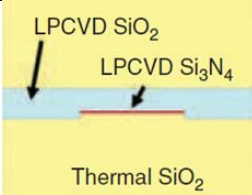
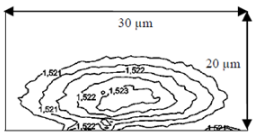
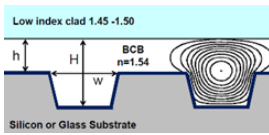
## 2.2 Low Loss Optical Waveguides

Optical waveguide is the fundamental building block in any photonics circuit. Single-mode optical waveguides on silicon photonics chips are naturally made from silicon [38]. Silicon waveguides have high index contrast and must be made small to maintain single-mode condition. However, the size mismatch between Si WG and fiber means the direct fiber coupling loss is 99%. In fact, a spot size converter must be added. Silicon Nitride ( $\text{Si}_3\text{N}_4$ ) waveguides have been demonstrated as a lower loss solution to Si WG [39]. While the NA is improved and loss is lower, it still has more than 90% coupling loss to fiber, which means a spot size converter is still needed. To promote direct fiber coupling, Fraunhofer IZM have developed gradient single-mode optical waveguides in doped glass [40]. The low index contrast waveguides can be designed with a large core size for direct coupling. However, a complex ion-exchange process is needed to create such waveguides. Polymer optical waveguides have been a staple of optoelectronics packaging,

particularly in the multimode domain, for their ease of implementation. Optical polymers from Dow Chemical have been used as single-mode waveguides with demonstrated low loss [41]. The low loss waveguides used in this thesis will use Dow Chemical polymer as the core material, and use glass itself as under cladding.

A quick comparison of the four types of optical waveguides covered is shown in Table 2.2.

**Table 2.2. Comparison of four types of optical waveguides by material**

Material	Silicon	Silicon Nitride	Doped Glass	Optical Polymer
Structure				
n @ 1.55 μm	3.48	1.99	1.51	1.49 – 1.6
Dimension	0.5 μm x 0.2 μm	2.8 μm x 0.1 μm	> 8 μm diameter	4 μm – 7 μm rectangle
NA	3.14	1.32	0.09	0.1 – 0.6
Fiber coupling	Requires spot size converter	Requires spot size converter	Direct coupling	Direct coupling

## 2.3 Out-of-Plane Turning Structures

Out-of-plane turning can be accomplished by adding another set of diffraction gratings on the interposer. However, the inherent loss of diffractive grating couplers (>1 dB) is inferior to that of a reflective device. For an interposer level solution, a traditional turning mirror is more practical.

A turning mirror could operate based on metallic reflection or total internal reflection (TIR) as defined by Snell's Law. A 45° turning mirror can be fabricated discretely by polishing, dicing, or molding [42], [43], [44]. While the discrete approach has proved valuable for quality assurance of

the turning mirrors, it usually accrue high cost due to the precision assembly required for each discrete component. Therefore, discrete approach is not suited for high volume manufacturing.

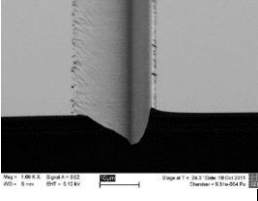
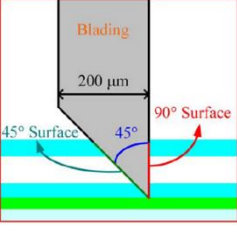
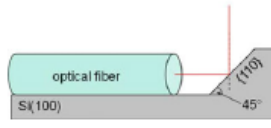
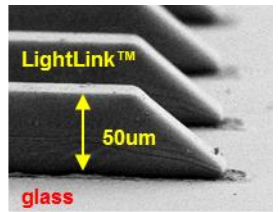
Integrated turning mirrors are most commonly fabricated by laser ablation, which create an angled cut to the planar fabricated optical waveguide [45]. While laser ablated turning mirrors have demonstrated low turning loss, the mirrors are formed serially, which limit their throughput. Several parallel photolithographic techniques have been employed to develop integrated micro-mirrors: grey scale mask [46], moving mask [47], and inclined lithography [48], [49]. Grey scale method utilizes a mask with stippling patterns, which correlates to a gradient exposure. For certain polymer materials, the material removed could be linearly proportional to the exposure dose. At this time, only positive-tone materials were proven as suitable candidates for grey scale mask lithography. However, the upfront cost to fabricate a stippled mask could be too high for small-scale prototyping, and stable behavior of the polymer could be very difficult to control.

Inclined lithography works by performing exposure with the substrate at a predetermined angle with respect to the direction of UV light. For large angles, such as the  $45^\circ$  turning in question, inclined lithography requires an index matching liquid to clear the critical angle, otherwise the UV light would be reflected. In addition, the alignment of mask to substrate during the inclined process must be preserved, which can be difficult to achieve without a special alignment stage that could also perform the tilt.

Moving mask method utilizes the same concept as grey scale exposure, except the gradient dose is translated into the polymer by moving the mask in a certain direction during exposure. Moving mask shares the same materials challenge as grey scale, but does not require an expensive mask. However, an exposure tool with programmable movement during exposure is needed. Fortunately,

such exposure tools are commonly available. For this thesis, moving mask lithography is chosen given the material and tools available.

**Table 2.3. Comparison of four existing types of out-of-plane turning methods**

Method	Laser Ablation	Dicing	Etching	Inclined lithography
Structure				
Throughput	Slow (serial)	Slow (serial)	Fast (parallel)	Fast (parallel)
Process	Laser tool	Dicing saw	KOH + mask	Double sided mask, immersion

## 2.4 Optical Fiber Alignment Structures

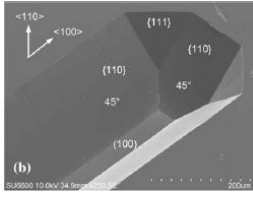
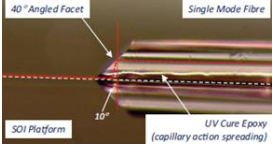
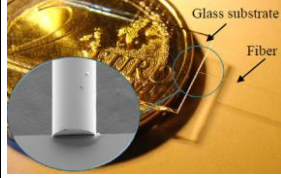

Laser assisted active alignment has been an industry standard to establish optimum positioning of the six-axis of freedom ( $x$ ,  $y$ ,  $z$ ,  $\theta_x$ ,  $\theta_y$ ,  $\theta_z$ ). Using active alignment, angle-polished fibers can be planar aligned to VGC at high efficiency [22]. Combined with laser joining, active alignment can even bond a fiber to a glass substrate directly [45]. However, active alignment is a costly process.

In order to qualify for passive alignment, up to four axes of freedom ( $x$ ,  $y$ ,  $\theta_x$ ,  $\theta_y$ ) must be restricted or clearly referenced, such that the alignment tool can accurately place the fiber. As mentioned in Chapter 1, optical fiber can be aligned either vertical to or in parallel to the interposer. Vertical passive alignment methods has been proposed by a through-silicon-via [37], or by a novel polymer wall [33]. There are two challenges with this approach: added package height and the

difficulty to control  $\theta_x$  and  $\theta_y$  using alignment structures less than 1 mm in height (mostly less than 200  $\mu\text{m}$ ).

Known for excellent dimensional stability and high precision, silicon optical bench (SiOB) has been used to accurately align optoelectronic components for more than 20 years [50]. Taking advantage of a highly anisotropic etch rate, silicon v-grooves capable of restricting four axis ( $x$ ,  $y$ ,  $\theta_x$ , and  $\theta_y$ ) can be wet etched along the (111) crystallographic plane in aqueous KOH (potassium hydroxide) solutions [51]. Glass can replicate the silicon v-groove shape by mechanical means such as grooving; however, only discrete components are available at the moment [52]. Polymer materials, such as Polyphenylene Sulfide (PPS), have been injection molded by US-CONEC to restrain  $x$ ,  $y$ ,  $\theta_x$ , and  $\theta_y$  [53]; however, the CTE mismatch of the ferrule with respect to the laser source makes large array alignment a concern. This thesis proposes to integrate glass micro-structuring to emulate silicon v-groove in SiOB.

**Table 2.4. Comparison of four existing types of fiber alignment structures**

Method	Silicon V-groove	Planar alignment on chip	Laser joining to interposer	Injection molding
Structure				
Build	Wet etched groove, epoxy cured	No etching needed, epoxy cured	CO2 laser joined, no epoxy	Injection molding
Restriction	$x$ , $y$ , $\theta_x$ , $\theta_y$	$y$ , $\theta_y$	$z$	$x$ , $y$ , $\theta_x$ , $\theta_y$
Alignment	Passive alignment	Active alignment	Active alignment	Passive alignment
Tolerance	1 dB: $\pm 2.5 \mu\text{m}$ xy 1 dB: 30 $\mu\text{m}$ z	1 dB: $\pm 2 \mu\text{m}$ xy 1 dB: 8 $\mu\text{m}$ z	1 dB: $\pm 3 \mu\text{m}$ xy No z (fiber joined)	Not reported

## 2.6 Summary

A survey of contemporary research and development efforts in board-to-board optical communication systems was provided in the beginning. Until recently, the research efforts have focused on multimode optical interconnections. However, multimode optics have inherent limitations in channel bandwidth and density. The maturation of silicon photonics with vertical grating couplers as a manufacturing-ready technology have ignited a wave of research in single-mode optical interconnections. Although single-mode optical communication systems have shown great promise in terms of channel bandwidth and density, the cost of packaging remains high and the fiber-to-chip coupling remains challenging.

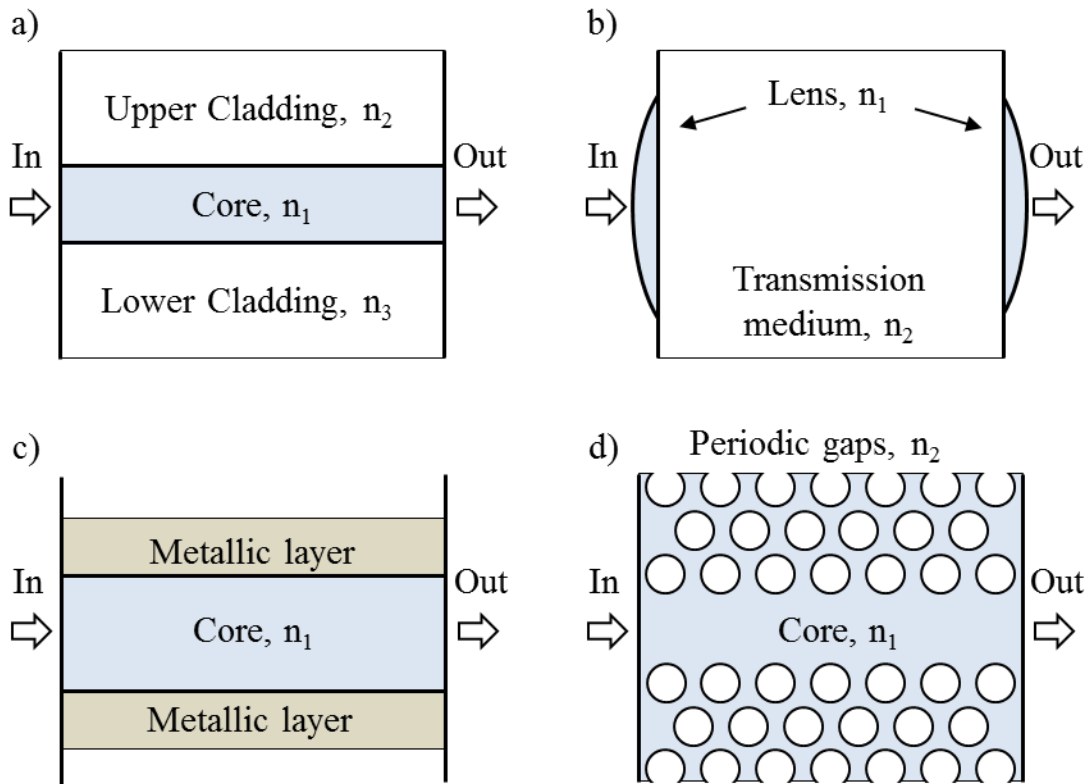
The second half of this chapter provided a focused review of contemporary research efforts to address the fiber-to-chip integration challenge by breaking it down to three levels consistent with the research objects presented in Chapter 1. First, different types of optical waveguides used at package level were compared. Second, a review of existing out-of-plane turning structures was provided. Finally, different ways to assemble optical fibers to an optical substrate was compared. The state-of-art metric used in Chapter 1 was compiled based on the review.



## CHAPTER 3

### OPTICAL WAVEGUIDES IN GLASS

Optical waveguides are the most fundamental building block in any optical system as they are responsible for routing light waves while preserving their power and preventing the waves from interfering with each other. Four types of waveguides are possible in a transparent medium such as glass: total-internal reflection (TIR) waveguides, lens waveguides, metallic waveguide, and photonic crystal waveguides. A simplified 2D illustration is shown in Figure 3.1.



**Figure 3.1. Four possible ways to guide light through glass with (a) TIR waveguide, (b) Lens waveguide, (c) metallic waveguide, and (d) photonic crystal waveguide**

Of the above, TIR waveguides are the most common, and will be studied extensively in this thesis. Lens waveguides and metallic waveguides are less common due to more complex design

and manufacturing requirements. They will also be investigated in this chapter. Given that manufacturability is a main theme in this thesis, photonic crystal waveguides requiring periodic patterning of nanometer-scale air holes in glass will not be explored.

TIR waveguides operate based on the well-known Snell's law:

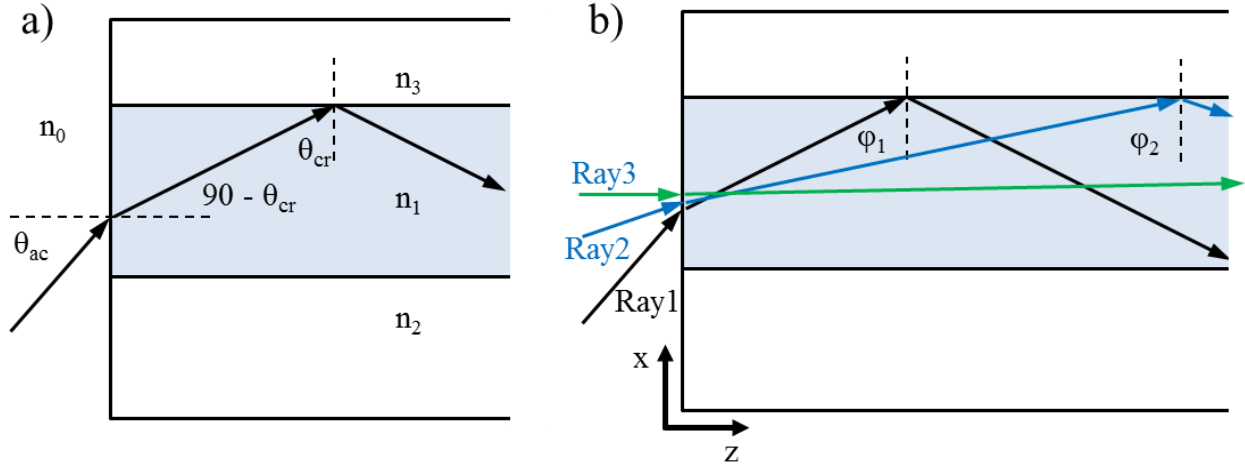
$$\frac{\sin \theta_1}{\sin \theta_2} = \frac{n_2}{n_1}, \quad (3.1)$$

which states the angles of incidence of a light wave traveling between two mediums is related to the refractive indices of each medium such that if light is traveling from a medium of a higher index,  $n_1$ , to another medium of lower index,  $n_2$ , the angle for which the light exits,  $\theta_2$ , will be greater than its entrance angle,  $\theta_1$ . Since a sinusoid cannot be greater than 1, there exist a critical incident angle,  $\theta_{cr}$ , such that the light will no longer propagate to another medium:

$$\theta_{cr} = \sin^{-1} \frac{n_2}{n_1}, n_1 > n_2. \quad (3.2)$$

Instead, all of the light will reflect within the first medium, hence the term “total internal reflection.” TIR waveguide operates by making sure the waveguide core has a higher refractive index than the surrounding cladding region. Due to its low propagating loss and ease of high volume fabrication, most commonly used optical fibers in the industry are based on TIR condition. Likewise, TIR waveguides are widely used at package and chip level photonics for their high density routing capabilities and compatibility to planar processing.

For a light wave to propagate through a TIR waveguide, it must incident the core within a certain angle, known as the acceptance angle  $\theta_{ac}$ , as shown in Figure 3.2a. This angle is more widely expressed as the **numerical aperture** (NA), of the waveguide. NA and  $\theta_{ac}$  are defined as follows:



**Figure 3.2. Guided wave propagation in a TIR waveguide with (a) the acceptance angle, the largest angle in which the wave can remain guided, and (b) a number of guided “modes” as defined by the reflection angle  $\phi_i$**

$$NA = \sin(\theta_{ac}) = \frac{1}{n_0} \sqrt{n_1^2 - n_2^2}. \quad (3.3)$$

In addition to entering the core within the numerical aperture, the wave front of the light must remain aligned as it reflects along the core. Only a finite number of such reflection angles,  $\phi_1$ , exists for a given core design. Therefore, depending on the core size, the index differences, and the wavelength of the light, there is only a finite number of propagating patterns, or modes, in which the light can take, as shown in Figure 3.2b. From this figure, intermodal dispersion (IMD) between different modes is easily visualized, as a mode with a smaller reflection angle will travel longer, hence arriving later than the fundamental mode, which has a reflection angle close to  $90^\circ$ . A single-mode waveguide, which is immune to IMD, can be made by proper selection of refractive indices and waveguide core dimension, such that only the fundamental mode can propagate.

Single-mode optical waveguides are needed for both horizontal and vertical transmissions through glass. They will be studied separately in this chapter. The turning structure that combines the two will be covered in the next chapter.

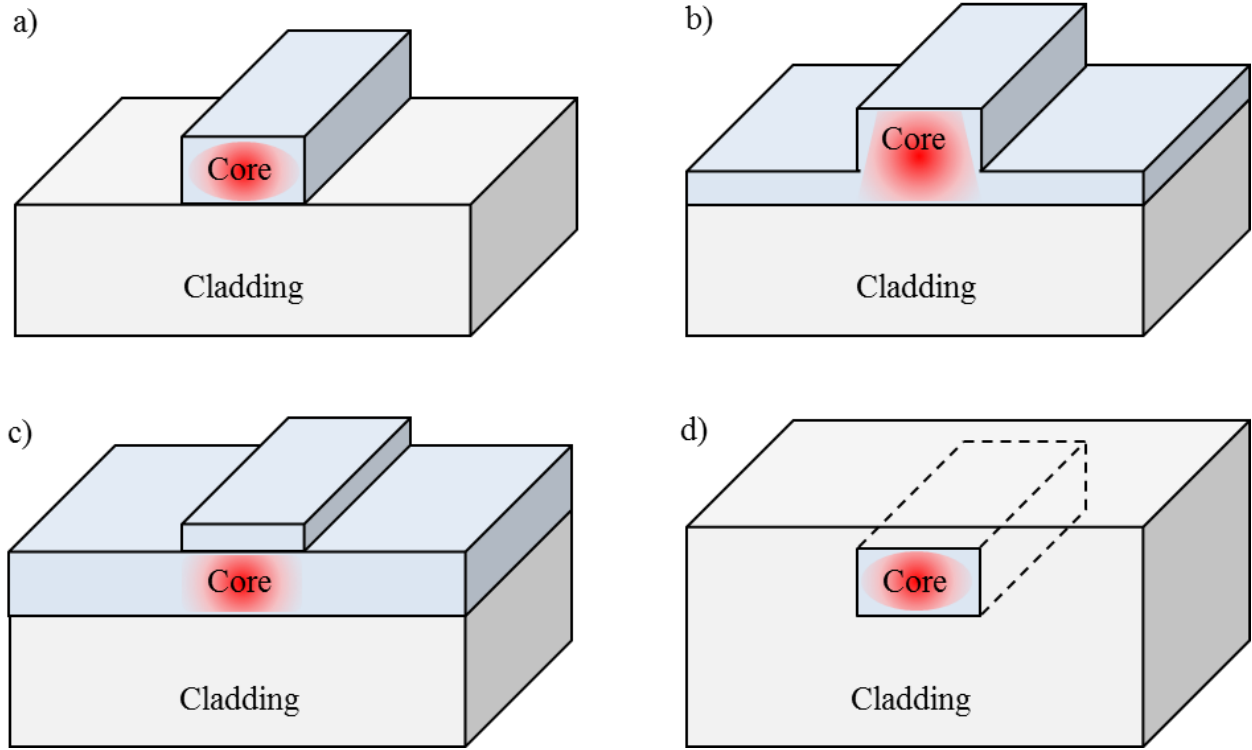
### 3.1 Horizontal Waveguides in Glass

Almost all horizontal waveguides in existence today are TIR waveguides due to their compatibility to planar lithographic process. TIR waveguides can be fabricated in many geometries, among which the popular choices are rectangular, rib, strip-loaded, and buried, as shown in Figure 3.3. A brief description of each geometry is as follows:

**Rectangular Waveguide** – Formed by deposition and patterning of core material on top of substrate cladding. The refractive index difference between the core and the substrate should be only a small percentage. If air is the upper cladding, the index difference between air and core will dominate the waveguide loss, specifically the sidewall roughness. Recently, very thin rectangular waveguides using silicon nitride have been developed to reduce the effects of sidewall roughness to waveguide loss [39].

**Rib Waveguide** – Formed by deposition of a thin layer of core material on a substrate. The waveguide area is defined by a rib on the thicker than the rest. The majority of the wave will be guided by a slight increase in effective refractive index of the core material under the rib. A large waveguide core is possible since the index difference can be made very small. For these reasons, rib waveguides are very popular for silicon photonics dies. The sidewall roughness of the rib is still a concern, but less so than rectangular waveguides [54].

**Strip-loaded Waveguide** – Similar to rib waveguides, a thin layer of core material was deposited on a substrate. The waveguide area is defined by the deposition and patterning of a strip whose index of refraction is lower than the core but higher than that of the surrounding area (air for example). This results in an increase in effective index under the strip similar to rib waveguides. Unlike rib waveguides, strip-loaded waveguides are not affected by sidewall roughness since the field is mostly confined in the core region [55].



**Figure 3.3. Common horizontal TIR based waveguide geometries. (a) Rectangular, (b) rib, (c) strip-loaded, and (d) buried**

**Buried Waveguide** – In a buried waveguide, the core is either completely buried in the cladding material, or immersed on three sides. The absence of cutoff region the dominant mode and the relative immunity to sidewall roughness means buried waveguides can have large core area with loss propagation loss. The fabrication of such waveguides have relied heavily on direct laser writing, which is low throughput [56]. Recently, buried waveguides in glass by ion exchange process was demonstrated by Fraunhofer IZM [40]. However, such waveguides are not suitable for optical modulation or coupling, as access to waveguide is difficult. Although the throughput was improved in this process, waveguide access and coupling remained a challenge.

In this thesis, rectangular waveguide is used for its compatibility to substrate level fabrication. The weakness of rectangular waveguide – namely the sensitivity to sidewall roughness, is addressed next by material design.

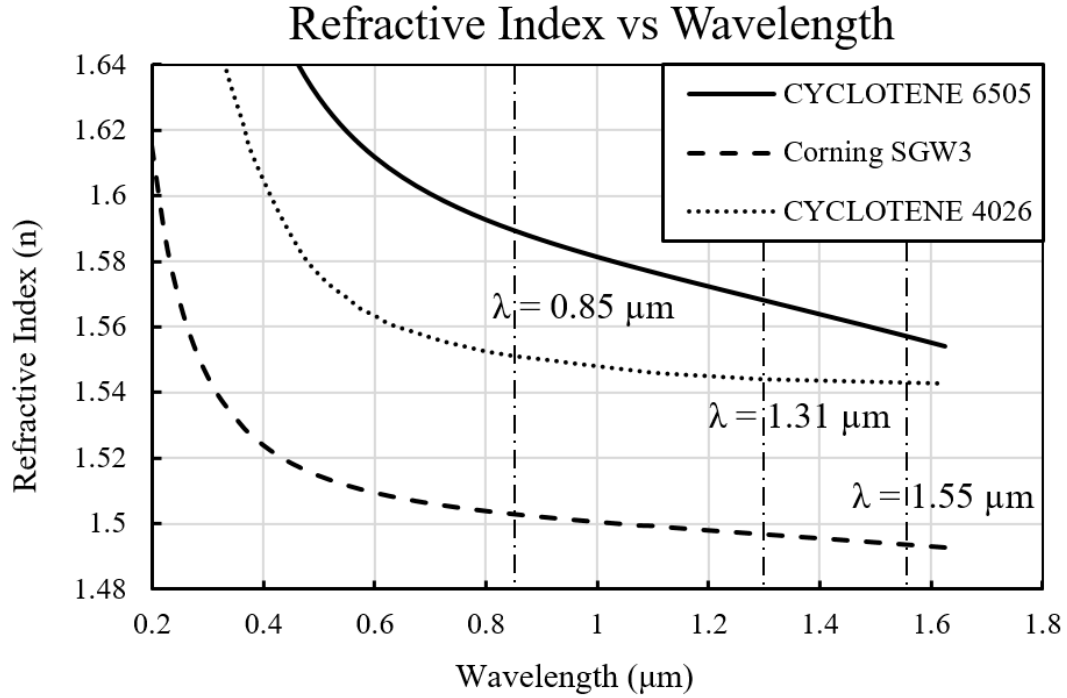
### 3.1.1 Waveguide Material Design

As mentioned in the beginning of this chapter, the precise geometry of the core region and the refractive indices of both the core and its surrounding regions must be precisely engineered to maintain single-mode operation. In this thesis, rectangular waveguide with glass as the under cladding / substrate is used. In order to address rectangular waveguide's sensitivity to sidewall roughness, a reflow-able polymer material is chosen to minimize surface roughness. Further, rather than using air as the upper cladding, another optical polymer with slightly lower refractive index is used, therefore maximizing the cross-section of the waveguide. The materials used in this thesis are the CYCLOTENE™ family of optical polymers based on benzocyclobutene (BCB) chemistry. BCB is chosen not just because of its reported low optical loss, but also because of its reflow ability and fine feature sizes. Two different types of CYCLOTENE™ materials are used – the positive toned CYCLOTENE™ 6505 for the waveguide core, and the negative toned CYCLOTENE™ 4026 for the waveguide upper cladding. The glass used in this thesis is the SGW3 (Semiconductor Glass Wafers with CTE = 3) by Corning Inc.

The refractive indices of optically transmitting materials change with respect to wavelength, which is known as the chromatic dispersion of the material. This relationship is defined by the Sellmeier equation defined as follows:

$$n^2(\lambda) = 1 + \frac{B_1\lambda^2}{\lambda^2 - C_1} + \frac{B_2\lambda^2}{\lambda^2 - C_2} + \frac{B_3\lambda^2}{\lambda^2 - C_3}. \quad (3.4)$$

The Sellmeier coefficients ( $B_i$ ,  $C_i$ ) are empirically determined by ellipsometry. For the optical materials used in this thesis, the coefficients are provided by the suppliers Corning Inc. and Dow Chemical, respectively. The refractive indices are plotted in Figure 3.4.



**Figure 3.4. Refractive indices of the optical materials used in this thesis as a function of wavelength, with three relevant wavelengths highlighted**

As shown in the figure above, the refractive index of the core material is always higher than that of cladding, thus satisfying TIR condition. The three wavelengths highlighted are common wavelengths for optical communication systems – 850 nm for VCSEL based multimode systems, 1310 nm and 1550 nm for WDM based single-mode systems, with 1550 nm as the most common. The index values at 1550 nm, which will be used throughout this chapter, are as follows:

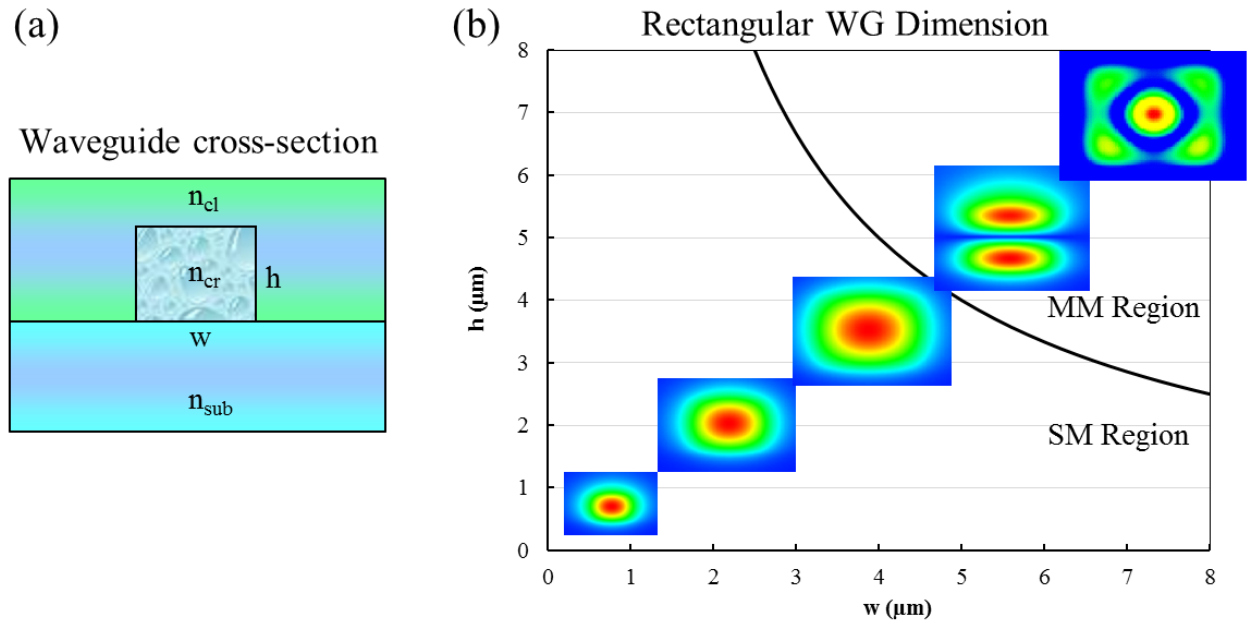
$$n_{cr} = 1.557 \text{ (CYCLOTENE™ 6505),}$$

$$n_{cl} = 1.543 \text{ (CYCLOTENE™ 4026),}$$

$n_{sub} = 1.494$  (Corning SGW3).

Another optical property of interest is the birefringence of the materials. Fortunately, CYCLOTENE™ polymer exhibit a birefringence of less than 0.0001, according to Dow, which is low enough to be negligible.

Once the materials are selected, initial modeling was done to determine the maximum dimension allowed while maintaining single-mode condition. The modeling was done using Optimode solver developed by Optiwave simulation software. A perfectly rectangular waveguide cross-section was assumed in this case. The simulation setup and the results are shown in Figure 3.5. From the modeling, the largest achievable single-mode waveguide with a square cross-section has  $w = h = 5.5 \mu\text{m}$ . In reality, however, the waveguide shape might not be rectangular. This will be covered next.



**Figure 3.5. Initial modeling of single-mode condition based on (a) ideal cross-section and (a) the divide between single-mode and multimode regions**



### 3.1.2 Waveguide Process Development

The optimized waveguide process is based on the standard procedure provided by Dow Chemical, but with modifications to work with glass substrate and tools in PRC's lab [57]. The detailed process is shown in Table 3.1. The achievable thickness is from 4 to 7  $\mu\text{m}$ , depending on the maximum spin speed attained. Spin speed of 1250 RPM resulted in 6  $\mu\text{m}$  height waveguide post-curing, whereas speed of 2000 RPM resulted in 5  $\mu\text{m}$  height.

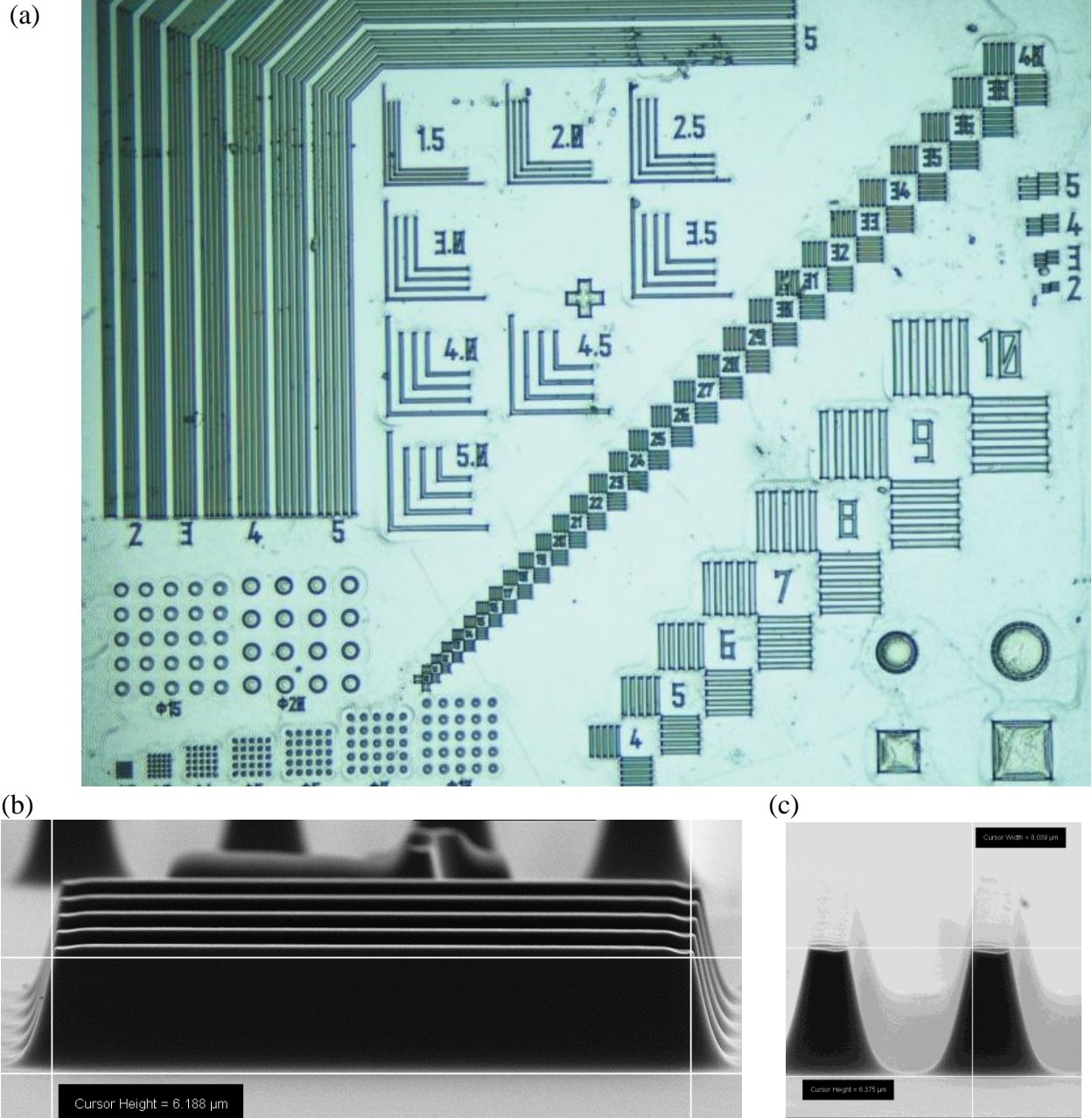
**Table 3.1 Optimized optical waveguide process condition for glass substrate**

Process	Step	Condition
Glass Substrate Cleaning	Plasma Clean	Plasma cleaner, O <sub>2</sub> , RF power 100 W, 100 C, 10 min
	Solvent Clean	Acetone, Methanol, IPA, DI water rinse, N <sub>2</sub> dry
	Drying	Hot plate, 100 C, 2 min
Surface Activation	Dispense Adhesion Promoter	Spin coater, 2000 RPM, 45 s
	Bake dry	Hot plate, 150 C, 90 s
Waveguide Patterning	Dispense CYCLOTENE™ 6505	Spin coater, 1250 RPM, 45 s
	Soft bake	Hot plate, 90 C, 90 s
	Lithography	i-line, 500 mJ/cm <sup>2</sup>
	Post-exposure delay	15 min
	Development	0.26 N TMAH, puddle, RT, 60 s

		DI water rinse
Curing & Descum	Thermal Set	Nitrogen oven, 130 C, 15 min
	Thermal Cure	Soft cure: 200 C, 100 min Hard cure: 230 C, 100 min
	Descum	Plasma cleaner, 4:1 O <sub>2</sub> :CH <sub>4</sub> , RF power 100 W, 100 C, 10 min

The adhesion promoter used is called AP900C, a Dow Chemical proprietary material developed specifically for the CYCLOTENE™ chemistry. The curing profile listed above will result in a slightly reflowed waveguide with a trapezoid cross-section. The curing condition has a very strong impact on the final shape of the waveguide, which will be explored later for making lenses. A test mask was used to assess the quality of the process. The results are shown in Figure 3.6.

The measured sidewall angle for a properly developed and cured waveguide is around 80°, which, along with height, limits the feature size achievable by the waveguide. A 4 μm width on mask begets a waveguide with top width of 1.78 μm and height of 6.2 μm as shown in Figure 3.6.  $6.2 * \tan(80) = 1.11$ , and  $4 - 2 * 1.11 = 1.78$ , thus the angle measurement and the waveguide dimension is consistent.



**Figure 3.6. Process development of optical waveguide core material using a mask to assess resolution. (a) Overall view from top, (b) SEM profile view of the 4  $\mu\text{m}$  line and space pattern, and (c) SEM cross-section view of the same 4  $\mu\text{m}$  pattern, showing trapezoidal shape. The waveguide height is approximately 6.2  $\mu\text{m}$ . The measured sidewall angle is roughly 80° normal to the surface of glass, which is consistent across the glass panel under the optimized process condition listed above**

### 3.1.3 Process-Aware Waveguide Design

With the process conditions set, the modeling for single-mode condition was redone with  $80^\circ$  sidewall angle. The modal condition was analytically determined using the effective refractive index of each mode. The condition is as follows:

$$n_{eff} < n_{cl}, \text{ Radiation mode.}$$

$$n_{cl} < n_{eff} < n_{cr}, \text{ Propagation mode.} \quad (3.5)$$

$$n_{cr} < n_{eff}, \text{ Forbidden.}$$

To satisfy the single-mode condition, one simply needs to determine the waveguide height and width where only the fundamental mode is propagating. Since the process condition is set, the height of the waveguide is assumed to be  $6.2 \mu\text{m}$ , with less than  $0.25 \mu\text{m}$  variance across panel. The effective index calculation as a function of waveguide width at the base was done using Optimode solver. The resulting maximum waveguide width, shown in Figure 3.7, is  $7 \mu\text{m}$ . The largest waveguide dimension is important in minimizing fiber coupling loss.

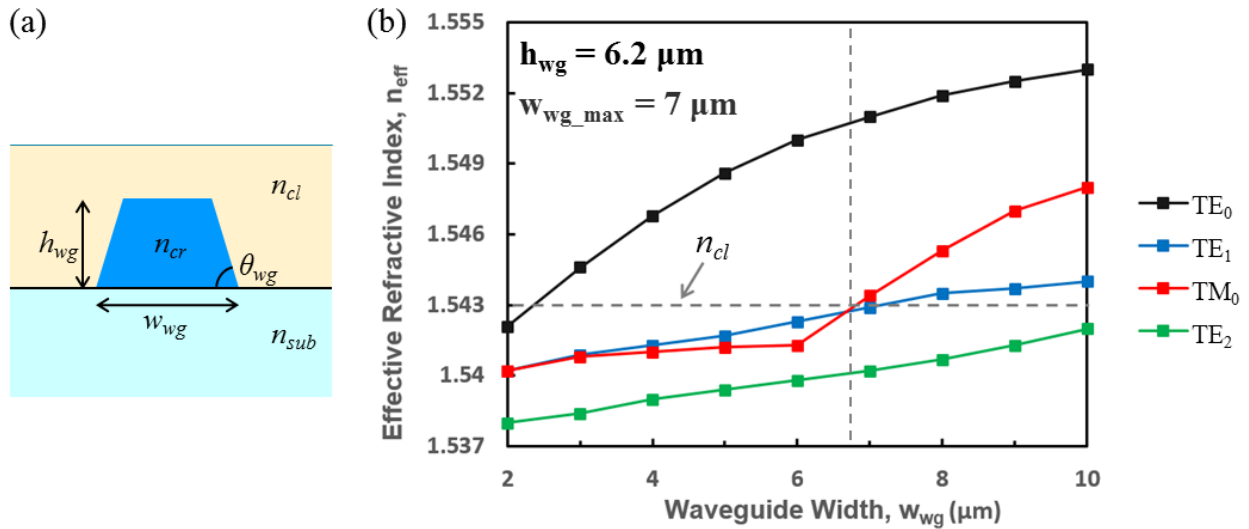


Figure 3.7. Modeling for single-mode waveguide dimension using effective index method

### 3.1.4 Waveguide Cladding Process Development

The cladding layer differs from the core in two significant ways. First, the cladding optical polymer is negative toned. This requires different exposure and development conditions. Second, the cladding material has been developed into a dry-film material compatible with standard substrate process as oppose to the liquid material requiring spin coating. This dry-film material is actually not called CYCLOTENE™ 4026, but code named 14-P005 as it is not commercially available [58]. However, it is based on the 4026 chemistry sharing the same refractive index, and it shall be referenced interchangeably in this thesis.

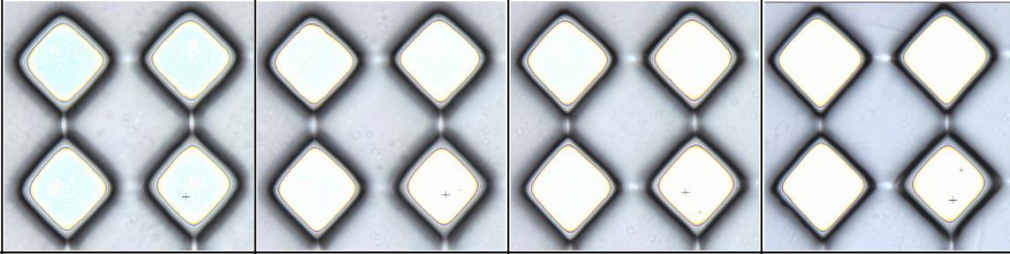
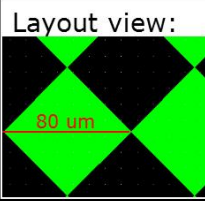
Normally, the cladding layer does not need to be patterned. However, due to its low electrical loss tangent and high thermal resistance, the 4026 material have also been used as the passivation opening for the electrical layer. In this thesis, the material will serve dual purpose as both passivation opening and optical cladding. The optimized process developed for PRC's lab setup is detailed in Table 3.2 [59]. The adhesion promoter is the same, AP9000c, as used for the waveguide.

**Table 3.2 Optimized waveguide cladding process condition for glass substrate**

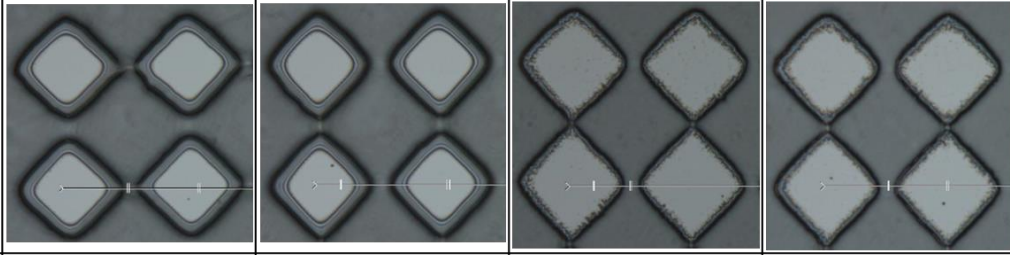
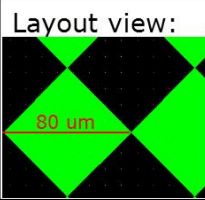
Process	Step	Condition
Glass Substrate Cleaning	Plasma Clean	Plasma cleaner, O <sub>2</sub> , RF power 100 W, 100 C, 10 min
	Solvent Clean	Acetone, Methanol, IPA, DI water rinse, N <sub>2</sub> dry
	Drying	Hot plate, 100 C, 2 min
Surface Activation	Dispense Adhesion Promoter	Rolled on with a rod

	Bake dry	Hot plate, 150 C, 90 s
Waveguide Patterning	Vacuum lamination	Meiki vacuum laminator, 90 C, 0.6 MPa, 90 s vacuum, 30 s pressure
	Lithography	i-line, 200 mJ/cm <sup>2</sup>
	Post-exposure bake	Hot plate, 90 C, 120 s
	Development	DS3000 immersion developer 35 C, 60 s, development RT, 60 s, rinse (no water)
Curing & Descum	Thermal Set	Nitrogen oven, 130 C, 15 min
	Thermal Cure	Soft cure: 200 C, 100 min Hard cure: 230 C, 100 min
	Descum	Plasma cleaner, 4:1 O <sub>2</sub> :CH <sub>4</sub> , RF power 100 W, 100 C, 10 min

One of the concerns for the dry film material as passivation is the minimum opening size. To optimize, a simple exposure ladder and development trial was performed with all other conditions remain unchanged. The results for the exposure ladder are shown in Figure 3.8, while the results for development trial are shown in Figure 3.9.

Exposure Time	10s	11s	12s	13s
Top view				
Layout view:				
Opening size Diagonal	Full: 48 um Partial: 58 um	Full: 50 um Partial: 59 um	Full: 51 um Partial: 60 um	Full: 52.5 um Partial: 62 um
Opening size Side	40 um	41 um	42 um	43.5 um

**Figure 3.8. Exposure ladder for passivation opening layer**

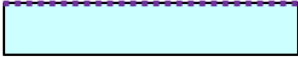




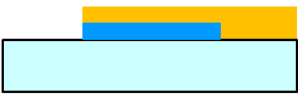
Condition	13s, immersion	16s, immersion	13s, puddle	16s, puddle
Top view				
Layout view:				
Opening size Side	47 um	47 um	52 um	51 um

**Figure 3.9. Development trial for passivation opening layer**

The optimum exposure time was determined by the exposure ladder experiment. The time was translated to power using a UV power meter, which measured the output of the Tamarack exposure tool used in PRC to be 14 mJ/cm<sup>2</sup>/s. The optimum range of 13 ~ 15 seconds is therefore translated to be 182 ~ 210 mJ/cm<sup>2</sup>. Two types of development methods were available for the 4026 material. The process trail above revealed that puddle based development method is more effective. However, since puddle method is not compatible with double-side substrate process, immersion technique was adopted in the end.

### 3.1.5 Design, Fabrication, and Characterization of Planar Waveguides

Fabrication and characterization of planar waveguides combined the process developed in the previous section. Shown in Figure 3.10 is an illustrated process flow.

Illustration	Process
	Activate glass surface
	Spin coat WG layer, soft bake
	UV exposure, development, soft cure
	Activate surface again for cladding
	Vacuum laminate cladding, soft bake
	UV exposure, development, hard cure

**Figure 3.10. Process flow for planar waveguide on glass**

Simple test structures were designed for a 100 x 100 mm<sup>2</sup> glass substrate to test the optical loss of the planar waveguides. Both single-mode and multimode waveguides were design in case there is an interest in using these materials for multimode purpose. The list of structures is shown in Table 3.3. The fabrication result is highlighted in Figure 3.11.



**Table 3.3 List of planar waveguide test structures**

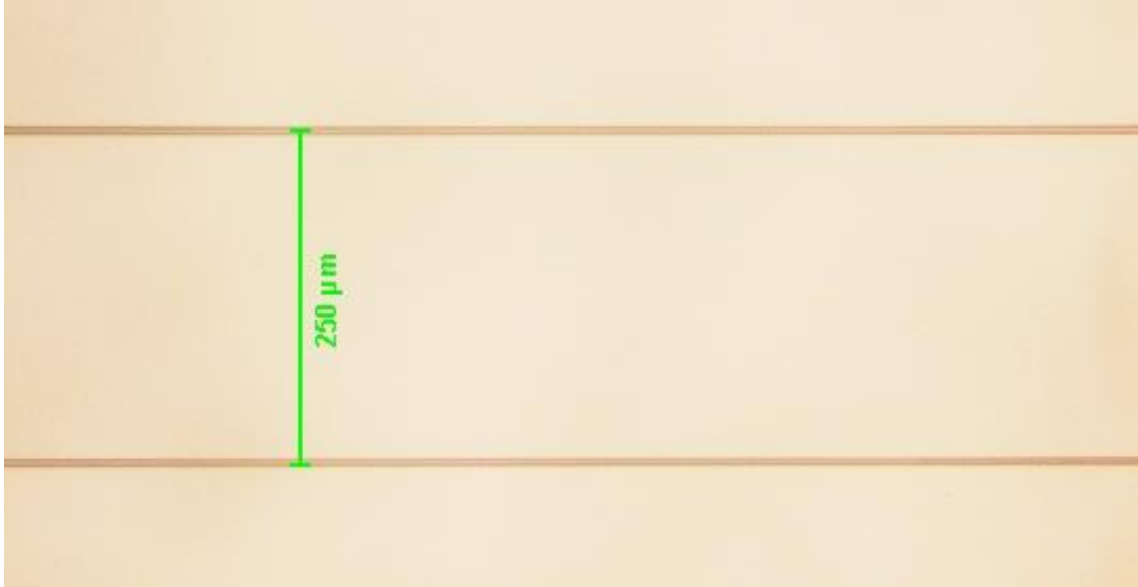
Structure	Description	Variation
Straight	10 cm long straight waveguides, in array of 5 at 250 $\mu\text{m}$ pitch	Width: 7, 16, 24, 32, 50 $\mu\text{m}$
S-turn	10 cm long waveguides with a S-turn at different radius	Width: 7, 16, 32 $\mu\text{m}$ Radius: 0.25, 0.5, 0.75, 1, 1.5 $\mu\text{m}$
Fan-in & fan-out	10 cm long 12 waveguide array, fan in from 250 $\mu\text{m}$ to 20 $\mu\text{m}$ pitch, then back to 250 $\mu\text{m}$	None

Optical measurement was performed using the setup illustrated in Figure 3.12. For standard cutback measurement of optical loss, a single-mode fiber input and multimode fiber output is sufficient. Using this method, an average power-loss is measured irrespective to the number of propagating modes in the waveguide, and the loss is given by

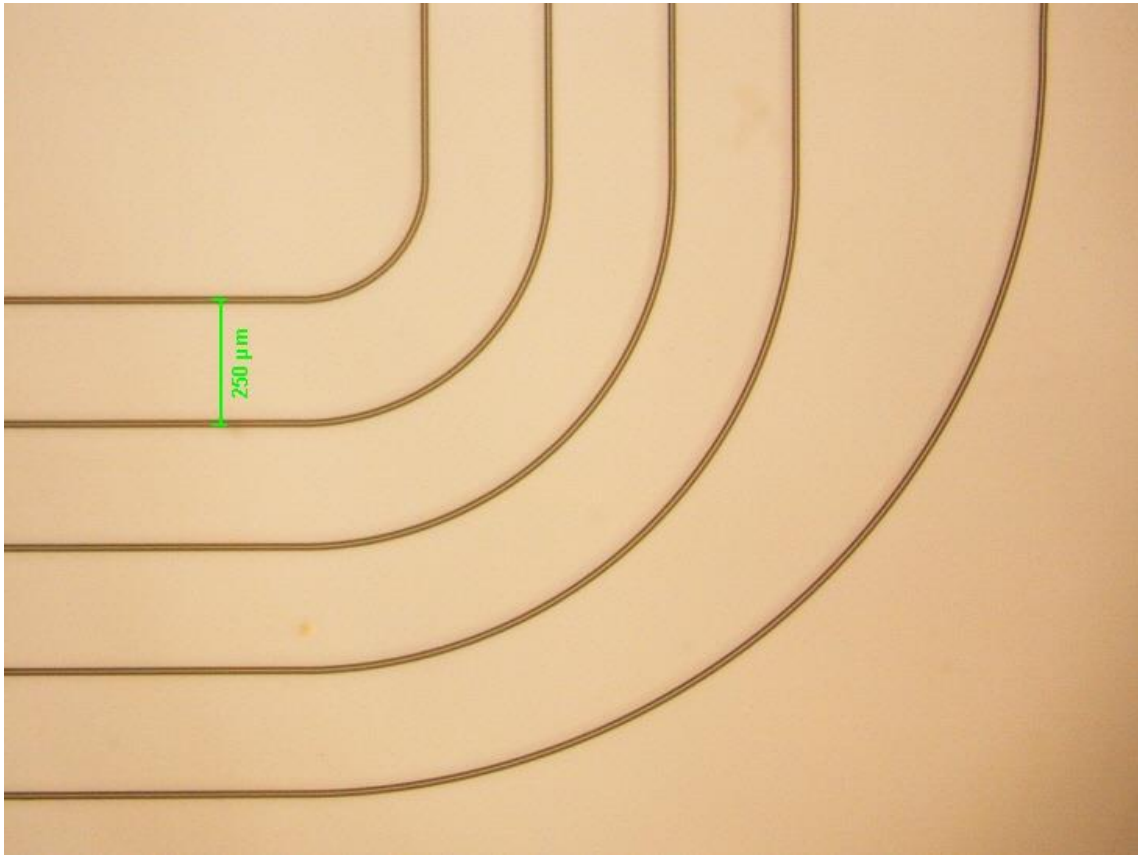
$$\text{Optical loss (dB)} = 10 \log\left(\frac{P_{out}}{P_{in}}\right). \quad (3.6)$$

This optical loss consist of both internal and interfacial factors. The internal factors include the material **absorption** loss and the **surface scattering** such as sidewall roughness. These factors are material and process dependent, and are usually scalable with respect to the length of the waveguide. On the other hand, the interfacial factors such as **coupling loss** and the **Fresnel reflection loss** are independent of the length of the waveguide. More discussions on the interfacial loss will be covered in the next section. Since the interfacial loss is independent of waveguide length, one can separate internal and interfacial optical losses by measuring the loss of a waveguide at different lengths and eliminate the extra loss at zero length.

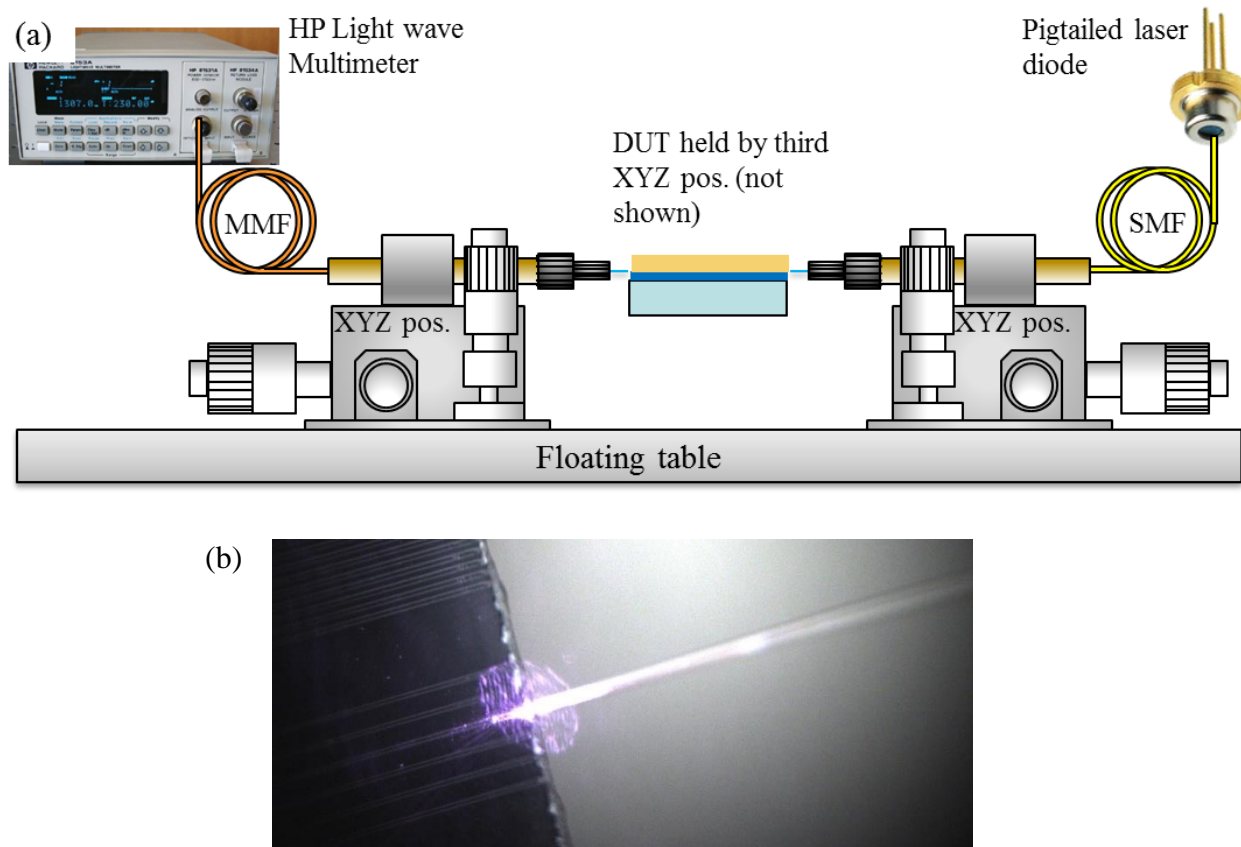
(a)



(b)



**Figure 3.11. Fabricated single-mode optical waveguides showing (a) straight and (b) s-turn structures**

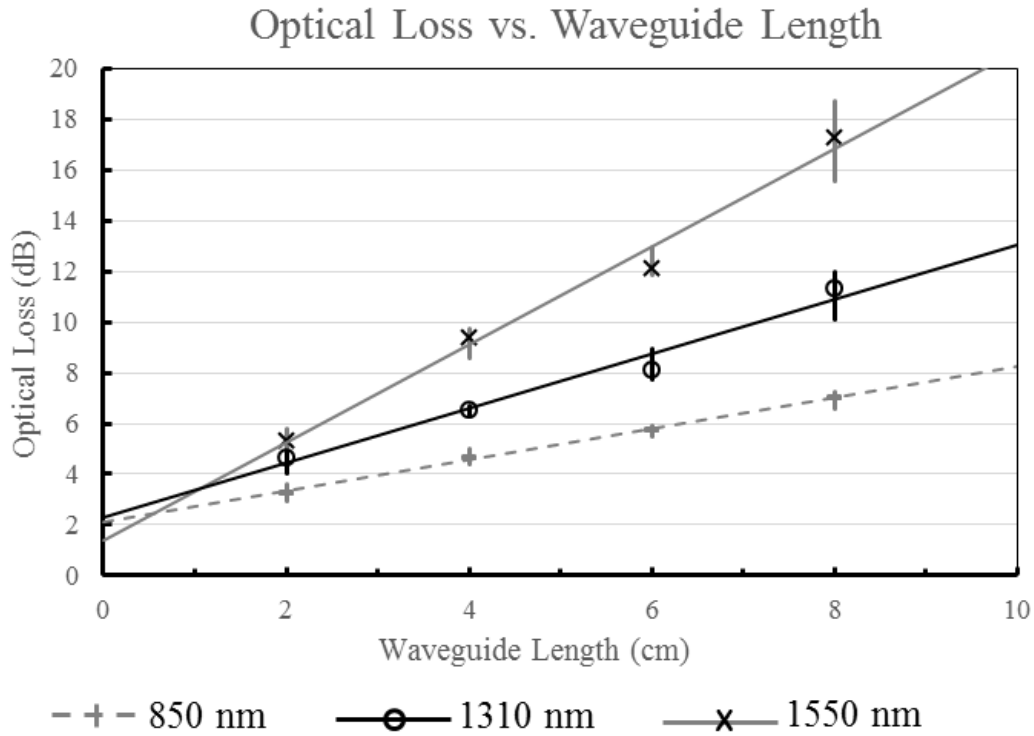


**Figure 3.12. (a) Illustration of waveguide loss characterization setup, and (b) input coupling from fiber to a waveguide showing guided light**

The cutback measurement was performed on a glass sample, and the results for straight waveguides are shown in Figure 3.13. The internal absorption and surface scattering losses are measured at three different wavelengths: 850 nm, 1300 nm, and 1550 nm. The loss increases with respect to the wavelength, as expected with the polymer material absorption. From the data, one can infer that, at 1550 nm, the waveguide loss is 2 dB/cm, with coupling loss of 1 dB. For on board applications where the length of the waveguide is typically much shorter than 1 cm, the coupling loss will dominate the optical loss. According to the datasheet provided by Dow Chemical, the waveguide loss should be lower by 50%. The higher measured loss is attributed to two process and measurement induced inaccuracies: 1) The cleanliness of the cleanroom oven during core curing

and 2) the sensitivity of the xyz micropositioner. During measurement, visible bright spots were observed at random intervals along the waveguide. These bright spots are caused by contamination during waveguide processing, which most likely came during curing, which takes the longest time. The xyz micropositioner is  $0.25\ \mu\text{m}$ , but since it is manually operated, the accuracy that can be achieved is around  $1\ \mu\text{m}$ .

It should be noted that the waveguide is in single-mode operation only at 1550 nm range, as more mode will propagation at lower wavelength under the same geometry.



**Figure 3.13. Optical loss of the waveguide, measured by cutback method**

### 3.2 Vertical Waveguides in Glass

Vertical optical waveguides, or “optical vias,” have not garnered nearly as much interest as planar waveguides due to the lack of application. After all, a majority of single-mode optical lasers and waveguides in existence today are all edge emitting. However, with the advent of vertical grating couplers, optical vias that allow vertical transmission of light through substrate at low loss are expected to gain wider usage. For this research, three types of vertical transmission through glass are explored: bare glass (no via), TIR waveguide (optical via), and lens waveguide (as in Figure 3.1.b). Since the distance of transmission is typically less than 0.5 mm, it is expected that most of the loss will come from interfacial loss, specifically the coupling loss and the Fresnel reflection. Gaussian beam theory is used to analyze the application space for each design.

#### 3.2.1 Gaussian Beam Analysis of Vertical Optical Transmission

In Gaussian beam theory, the power distribution of a single-mode light wave is approximated by a y-polarized Gaussian beam traveling in the z-direction, whose electric field is expressed as

$$E_y(r, z) = E_0 \exp \left[ \frac{-r^2}{r_g^2(z)} \right] \exp(-i\beta z), \quad (3.7)$$

where  $E_0$  is amplitude and  $\beta$  the phase constant of the beam. The “beam radius,”  $r_g(z)$ , at distance  $z$  from the source is

$$r_g^2(z) = r_0^2 + \left( \frac{\lambda z}{\pi n_0 r_0} \right)^2, \quad (3.8)$$

where  $r_0$  is the mode field radius (MFR) of the beam,  $n_0$  is the refractive index of the medium, and  $\lambda$  is the wavelength. The coupling efficiency between two guided mediums with MFR of  $r_0$  and  $r_1$  is calculated by finding the spatial overlap integral between the source and receiving fields. Taking

into account of misalignments, the efficiency is given by

$$\eta(x_0, z, \theta) = (1 - |\Gamma|^2) \kappa(z) \exp \left( -\kappa(z) \left\{ \frac{x_0^2}{2} \left( \frac{1}{r_0^2} + \frac{1}{r_1^2} \right) - \frac{x_0 \theta z}{r_0^2} + \frac{\pi^2 \theta^2 n_0^2}{2\lambda^2} [r_g^2(z) + r_1^2] \right\} \right) \quad (3.9)$$

where  $z$  is the distance between the two mediums,  $\theta$  is the radian angle between the two,  $x_0$  is the transverse displacement,  $\Gamma$  is the Fresnel reflection, and  $\kappa$  is defined as the “longitudinal efficiency” as it is a function of the variable  $z$  only [60]:

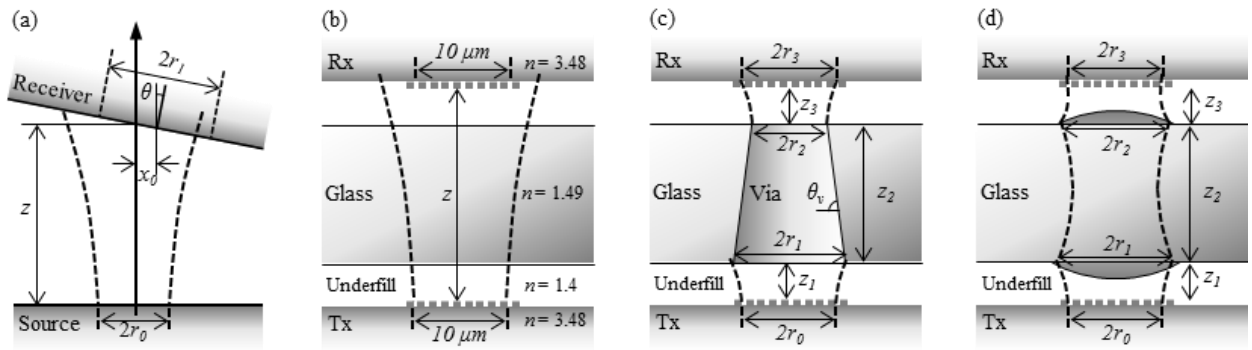
$$\kappa(z) = \frac{4r_0^2 r_1^2}{(r_0^2 + r_1^2)^2 + \lambda^2 z^2 / \pi^2 n_0^2}, \quad (3.10)$$

The Fresnel reflection is given by

$$\Gamma = \frac{n_i - n_f}{n_i + n_f} \quad (3.11)$$

where  $n_i$  is the refractive index of the initial medium and  $n_f$  the refractive index of the final medium.

The Gaussian beam coupling thus described is shown in Figure 3.14.a.



**Figure 3.14. Gaussian analysis of (a) vertical optical transmission with (b) no guide, (c) optical via, and (d) lens waveguide**

Figure 3.14.b, c, and d represent the cases in which the light goes through glass with no guidance, guided by an optical via, or guided by a lens waveguide, respectively. For the sake of comparison, a simple vertical coupling scenario is constructed where  $r_0 = r_1 = 5 \mu\text{m}$  are assumed from vertical grating couplers on die. The diffraction angle is assumed to be normal to the surface of the chips. The refractive index is taken to be 3.48 for silicon, 1.4 for the optical underfill, and 1.49 for the SGW3 glass.

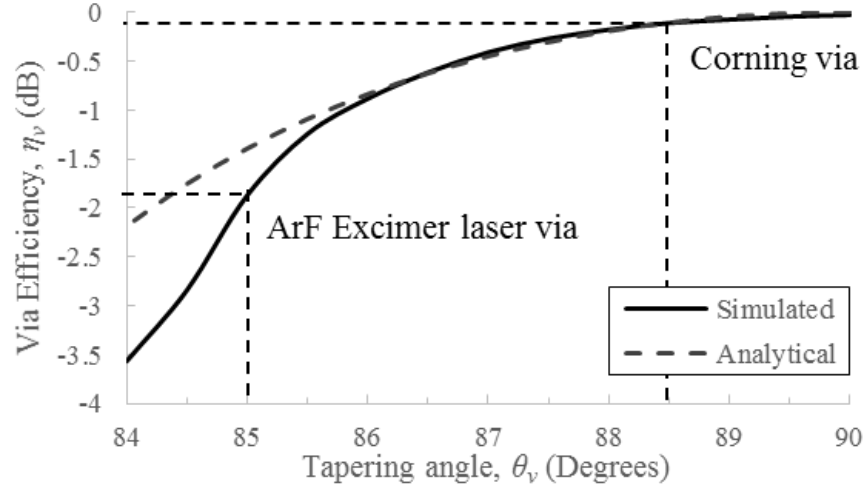
The coupling efficiency through bare glass,  $\eta_b$ , as a function of glass thickness  $z_2$ , die-to-glass spacing  $z_1$  &  $z_3$ , die-die misalignment  $x_0$ , and tilt  $\theta$  can be expressed as follows:

$$\eta_b(x_0, z_1, z_2, z_3, \theta) = (1 - |\Gamma_1|^2)(1 - |\Gamma_2|^2)\kappa(z_1 + z_2 + z_3) \exp\left(-\kappa(z_1 + z_2 + z_3)\left\{\frac{x_0^2}{2}\left(\frac{1}{r_0^2} + \frac{1}{r_1^2}\right) - \frac{x_0\theta(z_1+z_2+z_3)}{r_0^2} + \frac{\pi^2\theta^2 n_0^2}{2\lambda^2}[r_g^2(z_1 + z_2 + z_3) + r_1^2]\right\}\right). \quad (3.12)$$

The Fresnel reflections  $\Gamma_1$  and  $\Gamma_2$  are for glass-underfill interface and underfill-silicon interface, respectively.

### 3.2.2 Analysis of Optical Vias

Optical vias can be treated as a short fiber segment, such that the efficiency is now the product of  $\eta_{sv}$ ,  $\eta_{tv}$ , and  $\eta_{vr}$  which stands for source-to-via, through via, and via-to-receiver coupling efficiency, respectively. The through via loss is dominated by the scattering loss from via tapering, which could be determined by 3D Beam Propagation Method (BPM), using OptiBPM software from Optiwave. A survey of existing via forming process shows actual via tapering ranges from  $75^\circ$  to  $89^\circ$  [61]. The optical loss as a function of the taper angle is shown in Figure 3.15.



**Figure 3.15. Optical scattering and absorption loss as a function of via tapering angle**

For a highly vertical via formation technology such as Corning's proprietary process, the tapering loss is 0.1 dB. The typical intrinsic loss of an optical polymer is on the order of 1 dB/cm in C-band, which is 0.01dB at 100  $\mu\text{m}$  thickness. The through via loss can be approximated by

$$\eta_{tv}(\theta_v) = 1 - \left( (90 - \theta_v) \frac{\pi}{30} \right)^2, \quad \theta_v \geq 86^\circ. \quad (3.13)$$

The optical vias used in this thesis are Corning vias with  $89^\circ$  sidewall angle. Even though the tapering loss is low, the via diameter can vary by up to 10 microns depending on the thickness of glass. Therefore, careful selection of via entrance diameter is necessary for different thickness of glass to ensure optimum mode matching. An algorithm is developed where the average MFR between the source and the receiver is set at the center of the via. If the exit is too small, then the via exit mode field radius is matched to 80% of the receiver MFR:

$$r_1 = \frac{r_0 + r_3}{2} + \tan(\theta_v) \frac{z_2}{2}, \quad r_2 = \frac{r_0 + r_3}{2} - \tan(\theta_v) \frac{z_2}{2}, \quad (3.14)$$



*if  $r_2 < 0.8r_3$  then  $r_2 = 0.8r_3$  and  $r_1 = r_2 + \tan(\theta_v) z_2$ .*

The desired entrance radius can be calculated from the mode field radius  $r_l$  using Gaussian approximation of the fundamental mode. Once all of the parameters are determined, the overall coupling efficiency for vertical transmission through a via is

$$\eta_v(x_{0s}, x_{0r}, z_1, z_3, \theta_s, \theta_v, \theta_r) = \eta_{sv}(x_{0s}, z_1, \theta_s) \eta_{tv}(\theta_v) \eta_{vr}(x_{0r}, z_3, \theta_r). \quad (3.15)$$

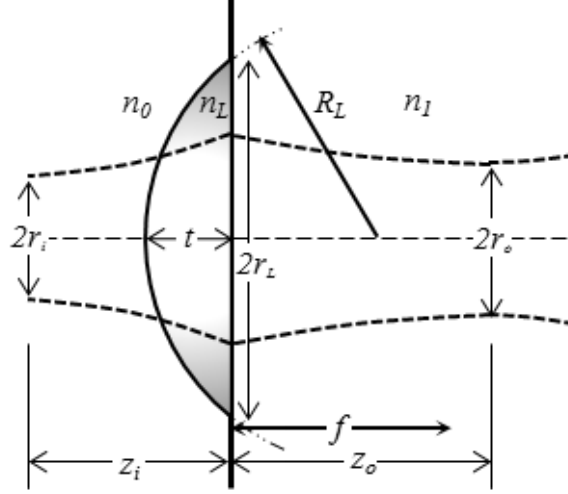
The efficiency is now independent of glass thickness. However, now two sets of alignment need to be considered: source-to-via, and via-to-receiver.

### 3.2.3 Analysis of Lens Waveguides

Plano-convex lens, which is half of a lens waveguide, acts as a phase transformer that matches the focal point of the lens and the wave front of the input beam, as illustrated in Figure 3.16. A detailed solution for focusing a Gaussian beam with a lens waveguide has been covered in detail elsewhere [62]. Only the single lens case will be presented here. A plano-convex lens is described by its focal length,  $f$ , refractive index  $n_L$ , and lens radius  $R_L$  by the Lens maker's equation

$$\frac{1}{f} = \frac{n_L - n_0}{n_0 R_L}, \quad (3.16)$$

where  $n_0$  is the refractive index of the region outside the lens surface.



**Figure 3.16.** Mode transformation of a Gaussian beam by a plano-convex lens

The dimension of a spherical lens on glass as defined by the thickness,  $t$ , and the radius  $r_L$  is related to the lens parameters by

$$R_L = \frac{t}{2} + \frac{r_L^2}{2t}, \quad r_0 < r_L < R_L, \quad t < r_L. \quad (3.17)$$

In actual fabrication a spherical shape for the reflow polymer lens is difficult to control if  $t \ll r_L$ , or  $t \approx r_L$ . Both cases are limited by the contact angle of the polymer material interface to glass. For the case above, the transformed longitudinal efficiency is

$$\kappa_L(z) = \frac{4r_0^2 r_i^2}{(r_0^2 + r_i^2)^2 + \left( \frac{\pi r_0^2 r_i^2}{\lambda} \right)^2 \left( \frac{1}{R(z)} - \frac{1}{f} \right)^2}, \quad (3.18)$$

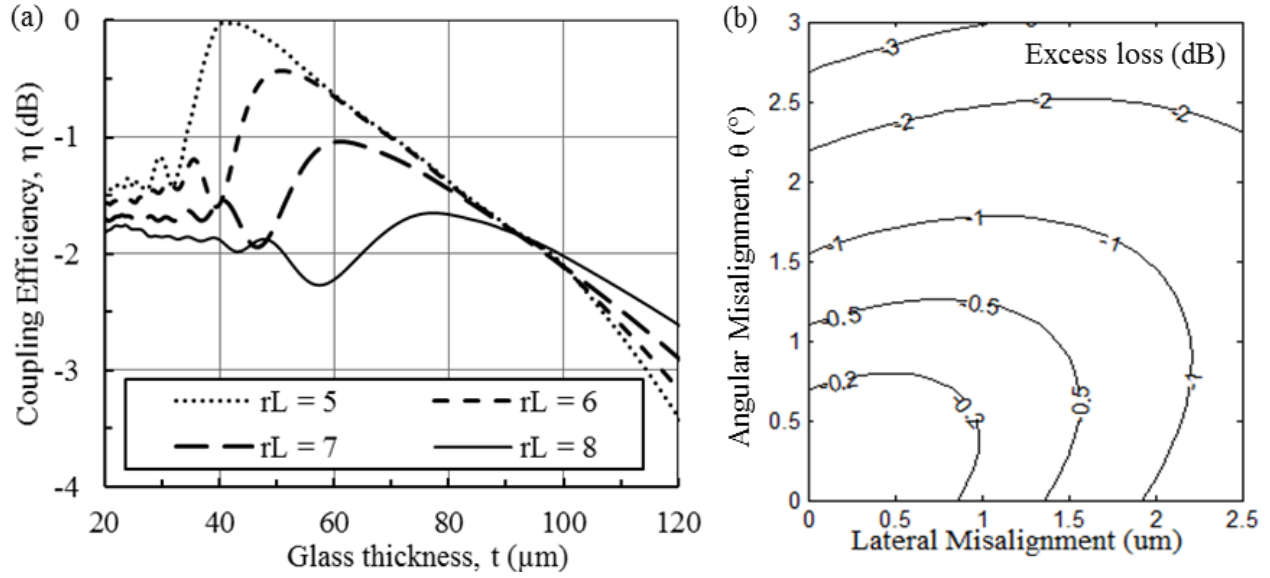
where  $f$  is the focal length of the lens and  $R(z)$  is the wave front radius, given by

$$R(z) = z \left( 1 + \left( \frac{\pi n_0}{\lambda z} r_0^2 \right)^2 \right). \quad (3.19)$$

The maximum efficiency at a specific distance  $z$  is achieved by matching  $R(z)$  to the focal length at point  $z$ , which will optimize  $\kappa_L(z)$ . Since the coupling is mode field matched, the highest efficiency can be achieved, with only Fresnel reflection to account for. However, unlike an optical via, a lens waveguide is very sensitive to glass thickness and die-to-glass space ( $z_1$ ,  $z_2$ , and  $z_3$ ). For each glass thickness, a specific lens waveguide is required. Further, for certain combinations of  $z$ , highest efficiency cannot be achieved. For example, if  $z_2 = z_3 = 20 \mu\text{m}$ , peak efficiency lens waveguide only exists for substrates with thickness less than around  $40 \mu\text{m}$ , as shown in Figure 3.17.a. As shown in the Figure, even though a lens with  $r_L = 6 \mu\text{m}$  is in focus for glass thickness of  $50 \mu\text{m}$ , the peak efficiency is only 90 % because  $z_2$  and  $z_3$  are too short. Also note the sensitivity to lens radius – a  $1 \mu\text{m}$  shift in lens radius can shift the focal point by  $10 \mu\text{m}$  and efficiency by 10 %. In fact, if the lens radius is  $> 7 \mu\text{m}$ , the lens waveguide becomes ineffective.

Simulated lateral and angular alignment tolerance of the source to the lens is shown in Figure 3.17.b. A strong interference is observed between the angle tilt and the lateral misalignment. Independently, the 1 dB point is  $< 2 \mu\text{m}$  in lateral side, and  $< 1.5^\circ$  in angular side. Both of these are worse than standard single-mode fiber coupling. In addition, the two lenses in the lens waveguide are required to align with each other. For these reasons, the application space of lens waveguides is very restricted.

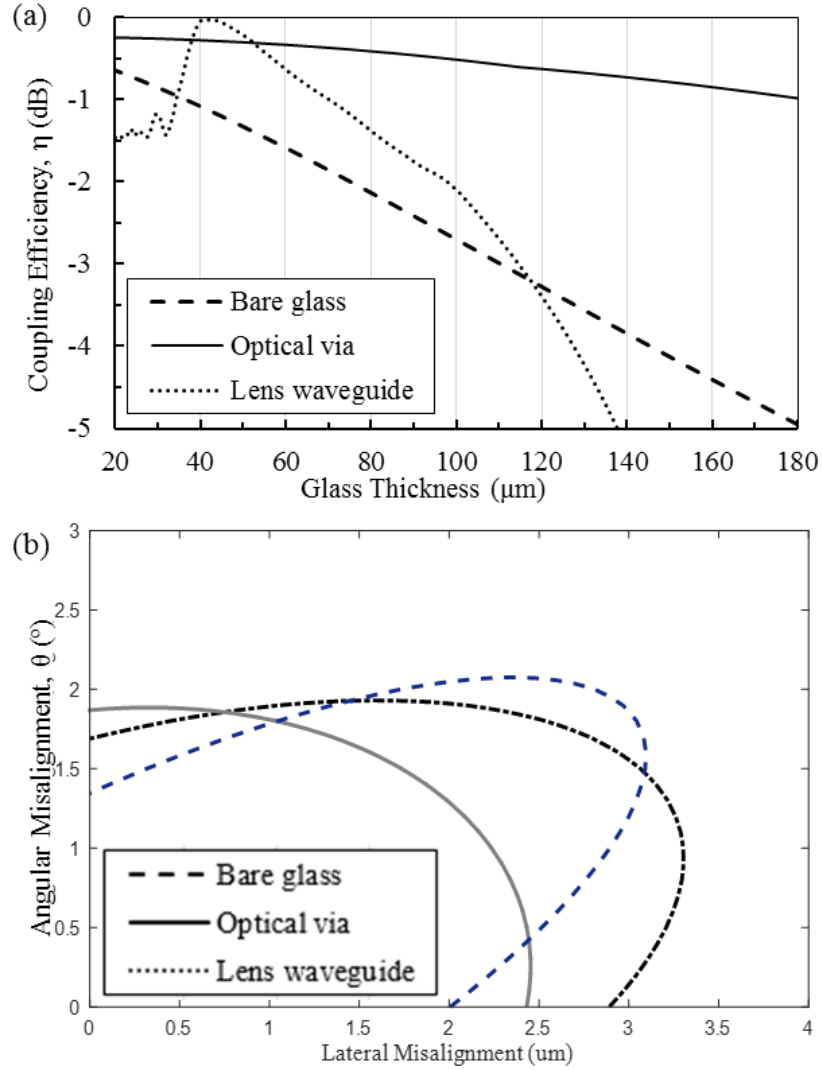
A side-by-side comparison of the coupling efficiency and alignment tolerances for bare glass, optical via, and lens-waveguide is shown in Figure 3.18. A  $10 \mu\text{m}$  diameter lens waveguide designed for  $40 \mu\text{m}$  thick glass is used in this study. The coupling efficiency with respect to the thickness of glass shows steady decay for bare glass as expected. Lens waveguide is able to achieve perfect matching at  $40 \mu\text{m}$ , but has a small window of operation. Optical via, on the other hand, retains low loss irrespective to glass thickness.



**Figure 3.17. (a) Coupling efficiency of lens waveguide as a function of substrate thickness at different lens radius, and (b) 2D lateral and angular alignment tolerance between lens waveguide and source**

The lateral and angular 1-dB tolerance is typically  $3 \mu\text{m}$  and  $1.5^\circ$  tilt for two single-mode fibers, which is reflected in the bare-glass case. With the introduction of optical vias, the angular alignment tolerance is improved slightly, to  $\sim 2^\circ$ , while the lateral alignment tolerance degrades to  $2.5 \mu\text{m}$  due to the requirement to align the source to the via. Lens waveguides, as mentioned previously, have a lower tolerance in both angular and lateral directions. Lens waveguides also have the strongest interference between lateral and angular misalignments comparing to bare glass and optical via transmission.

Optical vias have the best combination of low loss and relaxed alignment tolerance irrespective to glass thickness – in fact if the thickness of glass is greater than  $120 \mu\text{m}$ , optical vias are the only option capable of maintaining 3 dB coupling loss.



**Figure 3.18. Comparison of (a) coupling efficiency and (b) alignment tolerance of vertical optical interconnection**

### 3.2.4 Fabrication of Optical Vias and Lens Waveguides

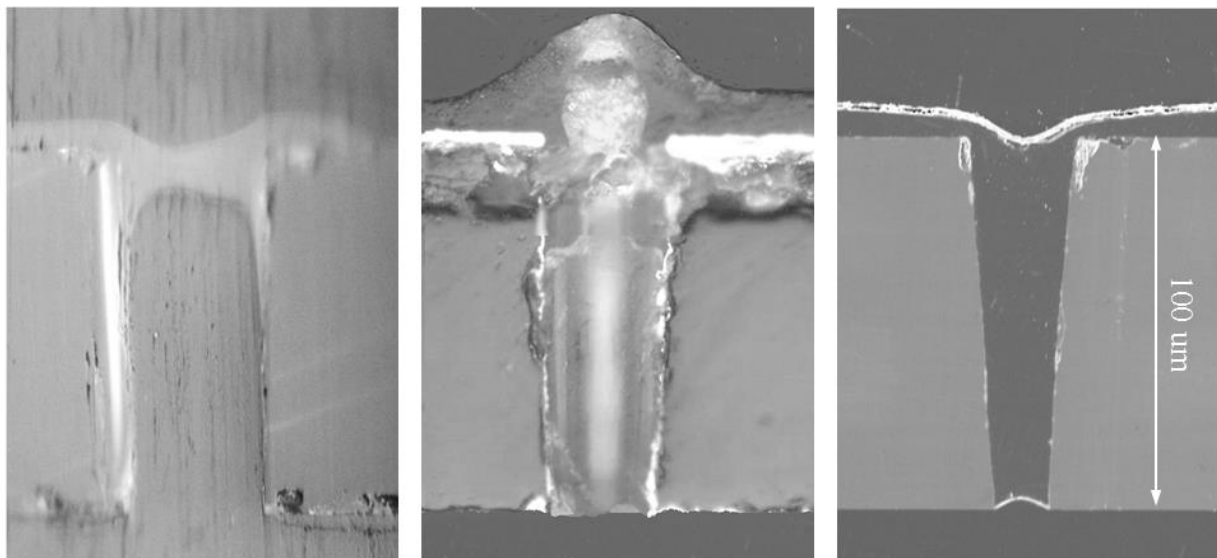
Optical vias are fabricated in ultra-thin (50 – 150  $\mu\text{m}$ ) glass substrate by polymer filling of through via holes using a vacuum-assisted deposition process. The through via holes are formed by Corning Inc. using their laser assisted etching process. Unfortunately, vias with diameter less than 20  $\mu\text{m}$  has yet been achieved to date, which means single-mode confinement vias do not yet

exist. The study to be presented here are done with a 30  $\mu\text{m}$  diameter via in a 130  $\mu\text{m}$  thick glass, in a 250  $\mu\text{m}$  pitch array, which was selected to match the pitch of an optical fiber array.

The optical material chosen is CYCOTENE<sup>TM</sup> 4026, which is already used as cladding for the planar waveguides. The via filling process must meet the follow two qualifications: 1) vias must be fully filled, (2) the via entrance and exit must be optically planar (i.e. dishing must be minimized).

Most liquid polymers have a tendency to tent over small openings. To induce via filling, a vacuum process based on the blind TSV filling process intended for electrical insulation is adopted [63]. However, this process requires a differential pressure between the air inside the vias and the air in vacuum to fill the vias. No such differential pressure is available for the through-via case, as the bottom sides are open. This challenge is addressed by forming a seal on the bottom side of the glass substrate.

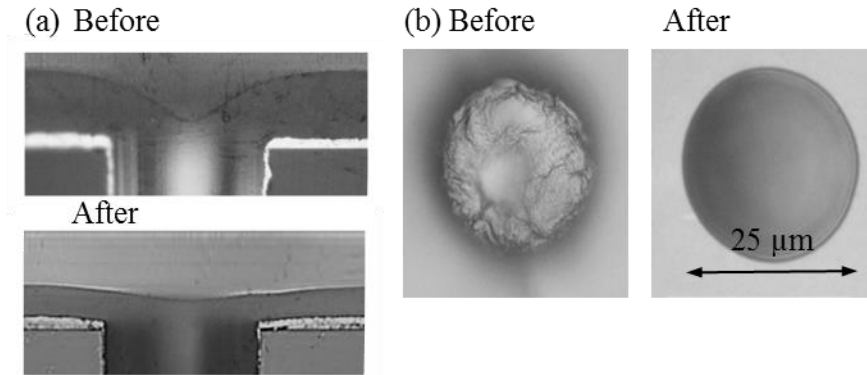
The initial sealing was created by mounting the glass with vias to a silicon wafer, and sealing the edges with wax. This technique is easy to implement, and allows iterative optimization of the vacuum parameters. The pressure was set to 0.04 torr, then the temperature and time were increased until complete filling was observed. If insufficient time was allotted, bubbles from the air in the via could be trapped near the top. Three examples of the filling trial are shown in Figure 3.19.



**Figure 3.19. Optical via filling optimization – from tenting to fully filled**

The exit end quality is poor due to contamination between the polymer and silicon support during breaking of the seal. Fortunately, the dry-film version of CYCOTENE™ 4026, which was described earlier, can be used to provide the sealing. Further, a vacuum press step was added after soft bake to reduce dishing. These process improvements are shown in Figure 3.20.

The resulting filled vias have optically smooth openings and less than 1 μm dishing. The filling result is very consistent. The yield of the optical via is assessed visually at both entry and exit side of 100 samples, is 98%. The surface roughness of the via entrance was measured using Veeco Atomic Force Microscope (AFM) on 10 of the vias. The average Sa was 51.9 nm, with a standard deviation of 37 nm. Since the roughness is more than an order of magnitude less than the wavelength of the light, it will not cause noticeable degradation.



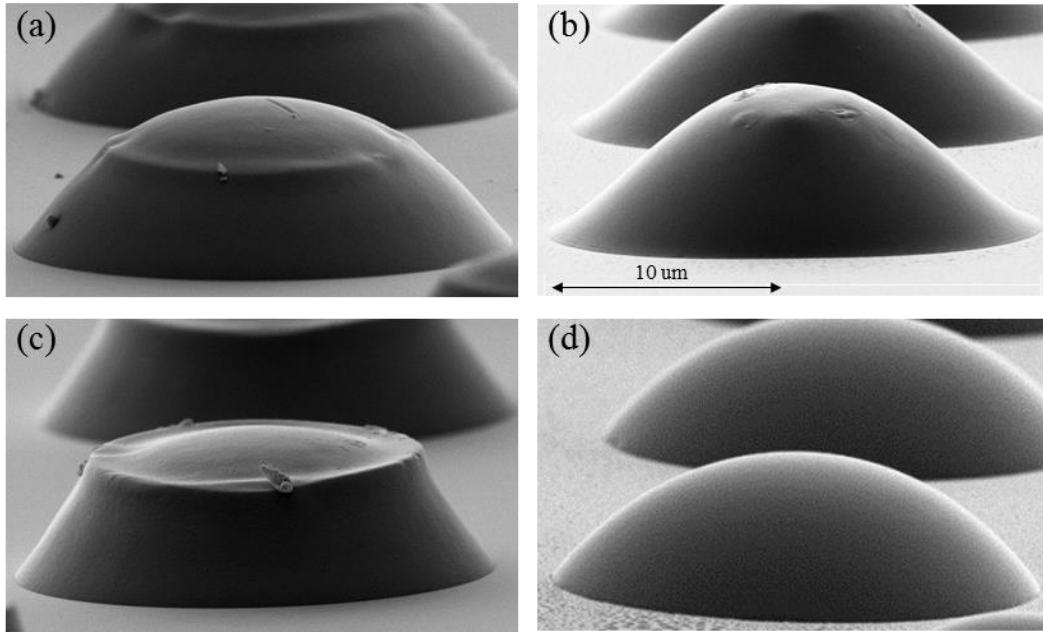
**Figure 3.20. Optical via (a) entrance and (b) exit quality optimization**

Plano-convex lens can be formed by reflow of optical polymer. The positive-toned CYCOTENE™ 6505 used as the core of the planar waveguide turns out to be an ideal candidate. The standard process flow for this material is already listed, in Table 3.1. The success in the reflow process hinges on an optimized curing condition. According to Dow recommendation, a combination of UV and thermal curing can yield drastically different sidewall profiles. A simple experiment was conducted to test this theory:

1. Standard process: 15-minute dwell at 130°C prior to ramping 230°C for full curing. This results in some reflow, and is used for waveguide formation.
2. UV cured: UV exposure was added prior to curing. Straight sidewall was observed. This result may come in handy later.
3. No dwell: The 15-minute hold time at 130°C is removed. Noticeably improved reflow was observed, but still not fully complete.
4. Elevated ramp: The sample was inserted in the oven at an elevated temperature (150°C), thus skipping the initial ramp-up completely. Complete reflow was achieved.

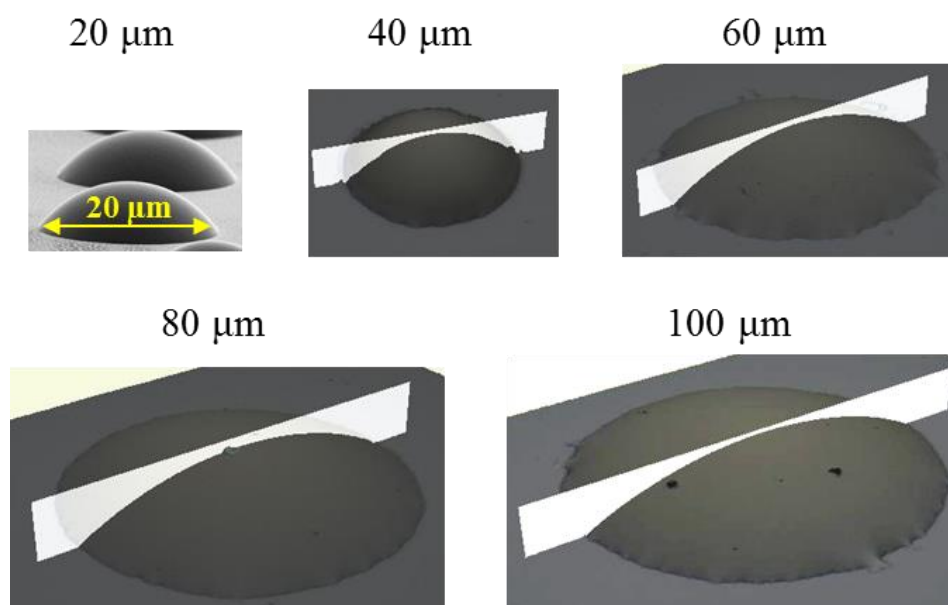
The results for all four conditions (20 μm diameter micro-lens array with 8 μm height) are shown in Figure 3.21.



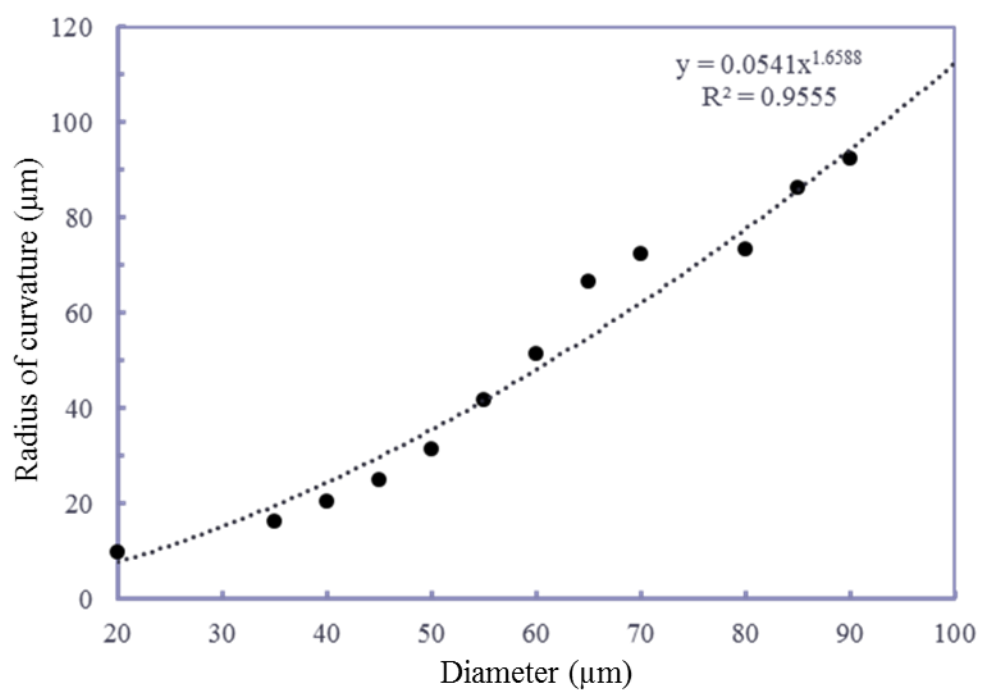


**Figure 3.21. Optical lens development with (a) standard process, (b) removal of holding time, (c) addition of UV cure, and (d) fast ramp at elevated temperature**

Since lens is reflowed from spin-coated polymer, the thickness of the lens is limited unless advanced multiple coating process is used. The 6505 material can only achieve 7  $\mu\text{m}$  thickness under single spin. As a result, the spherical reflow lens is limited by the contact angle of the material to glass. To test this limit, spherical lens with diameter from 10  $\mu\text{m}$  to 100  $\mu\text{m}$  were fabricated using the same process, as shown in Figure 3.22. Lens with diameter less than 15  $\mu\text{m}$  shows poor adhesion to glass, while a non-linear relationship is observed between the radius of the lens and the radius of curvature of the lens, as shown in Figure 3.23. As shown, the radius of curvature is roughly equal to the radius of the lens for small lens, but extends to close to twice the radius of the lens for a larger lens.



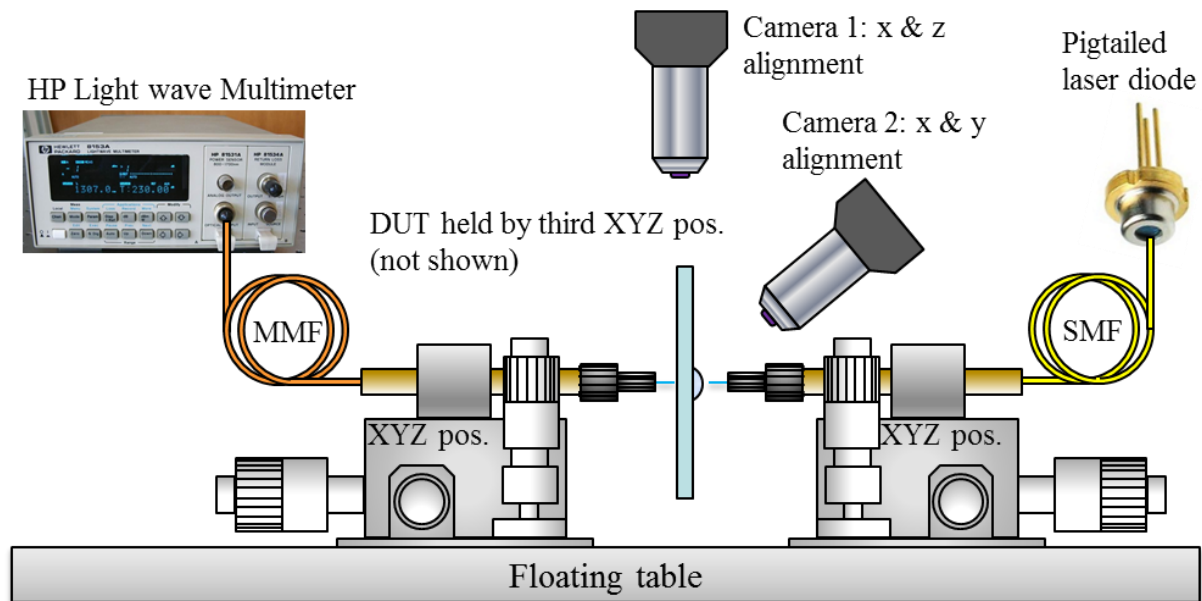
**Figure 3.22.** Spherical lens with diameter ranging from 20 to 100  $\mu\text{m}$ , with profile measured across the centerline



**Figure 3.23.** Correlation between radius of curvature of lens and lens diameter

### 3.2.5 Characterization of Vertical Optical Transmission

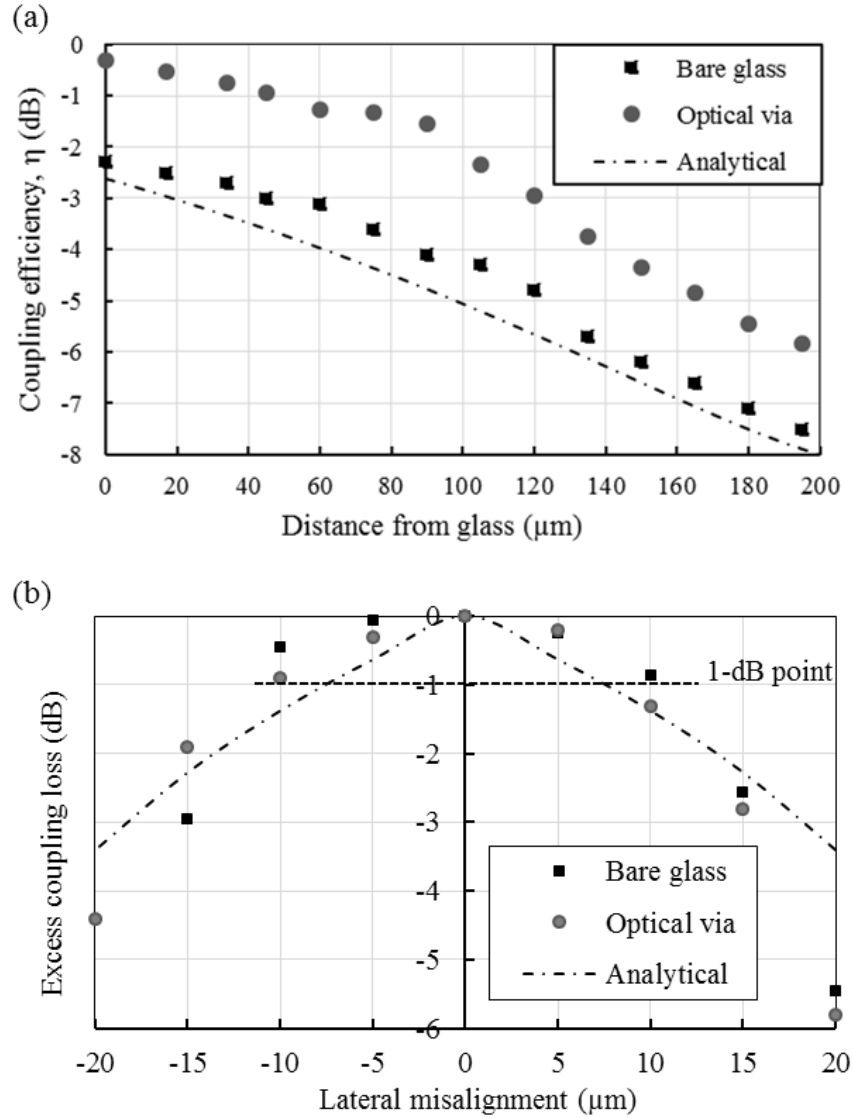
To validate the analytical model, the fabricated optical vias and lenses were measured for coupling efficiency and tolerance using the setup shown in Figure 3.24. In this setup, both input and output fibers were mounted on a Newport 561D ULTRAlign™ stage with x, y, z,  $\theta_y$ , and  $\theta_z$  control, and 1  $\mu\text{m}$  sensitivity micrometers. The Device Under Test (DUT) is held by a third stage, Newport 462 stage with only x, y, z control, but with high sensitivity (0.25  $\mu\text{m}$ ) micrometers installed. Three laser wavelengths are used: 850 nm, 1310 nm, and 1550 nm. Two microscopes, one on top and another on the side, were mounted to assist with fiber alignment. A camera was mounted off axis, looking at the x-y plane, as shown in the figure. The limited resolution of the microscope and the camera can only bring the DUT close to the fibers. Manual scanning of the axis for peak power must be followed for each sample.



**Figure 3.24. Measurement setup for vertical optical transmission through glass**

Coupling efficiency of a 30  $\mu\text{m}$  optical via in 130  $\mu\text{m}$  thick glass was measured using SMF input and MMF output, with an 850 nm laser, and compared against the same measurement done on bare glass. Since only one glass thickness is available, successive measurements were made with the input fiber pulled back to mimic longitudinal coupling loss. The lateral misalignment was taken at 20  $\mu\text{m}$  gap between the output fiber and DUT. Angular misalignment was not measured. The resulting coupling loss data is shown in Figure 3.25. Also plotted are the analytical models based on Eq. 3.15.

Since optical via dimension is not single-mode, the coupling loss and alignment tolerance loss is not expected to match Gaussian beam analysis. The loss though optical via measured at via exit was less than 0.5 dB as compared to more than 2 dB from bare glass. The measured loss was higher than analytical model, which is likely due to the different NA as light travels through glass. The lateral alignment tolerance doesn't show much difference between optical via and bare glass, which means the addition of via does not degrade the alignment tolerance as one might suspect.



**Figure 3.25. Optical characterization results for vertical transmission**

### 3.3 Summary

Single-mode optical waveguides both planar to the surface of glass and traveling through glass have been studied in this chapter. The planar waveguides on glass consists of a trapezoidal core in CYCLOTENE™ 6505 optical polymer covered by a cladding in CYCLOTENE™ 4026 optical polymer. The low refractive index difference between the core and upper cladding enables a large

waveguide core for single-mode propagation. Cutback optical loss measurement of the waveguide shows 2 dB/cm of loss with about 1 dB of coupling loss at 1550 nm, the wavelength of interest for single-mode operation. The high propagation loss is likely due to surface defects.

Gaussian beam analysis is used to understand the coupling efficiency and tolerance of three different methods of optical transmission through glass: bare glass transmission, optical via transmission, and lens waveguide transmission. While bare glass transmission is sufficient for very thin glass at 30  $\mu\text{m}$  thickness, the beam divergent becomes too wide when the glass gets thicker. Optical via, if it can be fabricated, provides optical confinement by total internal reflection irrespective to glass thickness. Given the right condition, lens waveguide can be designed to achieve 100 % coupling efficiency; however, any variation in fabrication will cause the efficiency to drop off. Considering the combination of efficiency and tolerance, optical vias provide the most flexibility for a given design. Optimized fabrication optical via and lens waveguide in glass are presented, achieving optical quality surface in both cases. The coupling loss and tolerance of optical vias are measured using butt coupling method. Only a slight advantage is observed between optical vias and bare glass transmission.

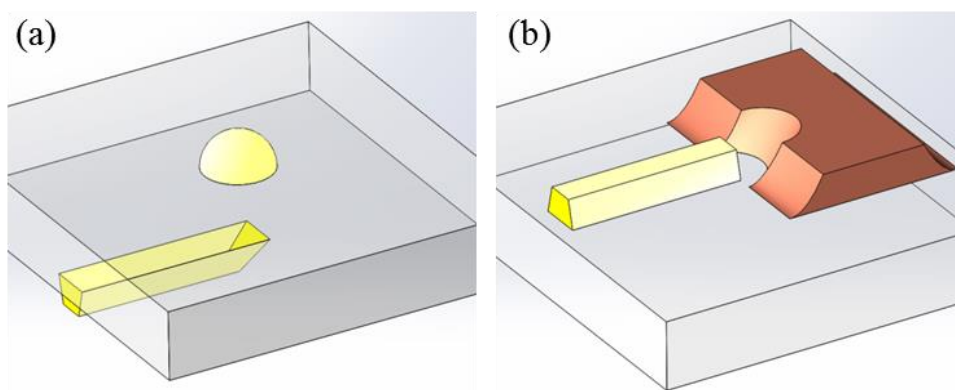
Planar polymer waveguides in glass have proven to be a scalable and low loss solution to optical routing from chip to fiber. Vertical optical transmission by via or lens faces fundamental challenges in fabrication and has a narrow design window. If the glass is thin enough, no confinement is needed.

## CHAPTER 4

### OUT-OF-PLANE FIBER-TO-CHIP COUPLING IN GLASS

Optical waveguides and vias presented in Chapter 3 are, by themselves, useful interconnects, but they are limited to axial coupling of light without an out-of-plane turning structure. The design and development of out-of-plane turning structures, their integration with optical waveguides, and the exploratory work on fiber alignment grooves will be presented in this chapter. For this thesis, moving mask lithography will be used to fabrication planar aligned and processed out-of-plane turning structures on glass.

Two types of turning structures are proposed in this thesis: turning by total-internal-reflection (TIR) of polymer-air interface, or turning by a metallic mirror, as shown in Figure 4.1. In both structures, the turning area is built by moving mask lithography.



**Figure 4.1. Out-of-plane turning by (a) Total Internal Reflection (TIR) and (b) metallic turning mirror**

The TIR structure, conceived first relies on either a plano-convex lens or an optical via for vertical light guiding after turning. As will be shown later, this design is challenging to implement and requires precise alignment of lens to turning waveguide on the bottom side. The metallic

turning structure was proposed to address the challenges of TIR turning structure. Both will be presented in detail in this chapter.

#### 4.1 Moving Mask Lithography

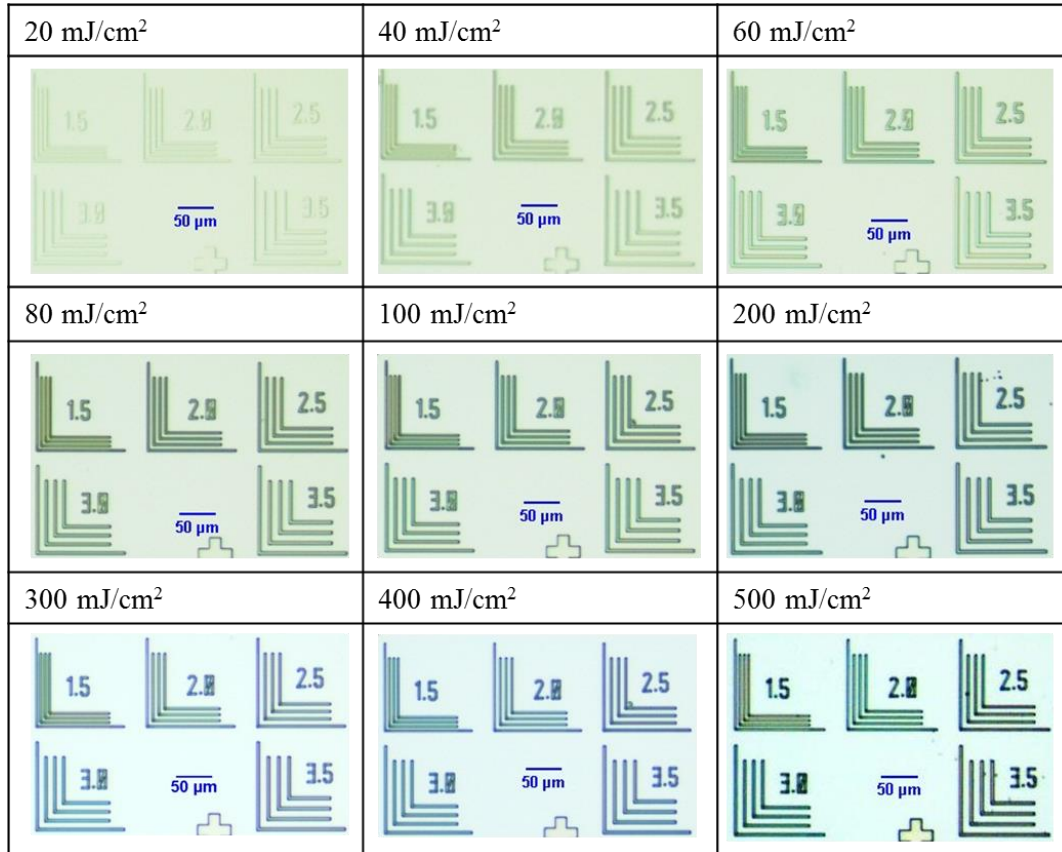
Moving mask lithography is a planar lithography technique that generates an oblique structure by horizontal mask translation during exposure. The mask translation corresponds to a gradient exposure dose experienced by the polymer in the direction of translation. If the polymer used has a linear height profile with respect to exposure dose, the polymer is expected to have an oblique structure upon development, closely matching the input translation.

The first step in developing the moving mask process is to determine the relationship between polymer height and the exposure dose. The polymer material used, as mentioned in Chapter 3, is the CYCLOTENE™ 6505 positive toned BCB material. For process development, a 4" silicon wafer was prepared following the condition detailed in Table 3.1. After coating and drying, UV exposure was performed using an i-line (365nm) projection aligner (UX-44101) from Ushio Inc., Japan, for a series of exposure doses of 20, 40, 60, 80, 100, 200, 300, 400, and 500 mJ/cm<sup>2</sup>. After exposure, the post exposure delay was administered before development by TMAH (2.38%) using a one-minute single puddle method. Finally, the waveguide top view and step heights before curing were measured by a mechanical surface profiler. The top view of all of the points are shown in Figure 4.2. The measured step height increases proportionally until 400 mJ/cm<sup>2</sup> and remains constant at 500 mJ/cm<sup>2</sup>; therefore, it is concluded that the exposed material is completely cross-linked at the dose of 400 mJ/cm<sup>2</sup>. A linear fit of waveguide height,  $h$ , and the exposure dose,  $D$ , using the data up to 300 mJ/cm<sup>2</sup> has a 0.995 correlation:

$$w = 0.0167D. \quad (4.1)$$



The linear fit with the measured data is shown in Figure 4.3. Also shown is the profile of the waveguide at two doses.

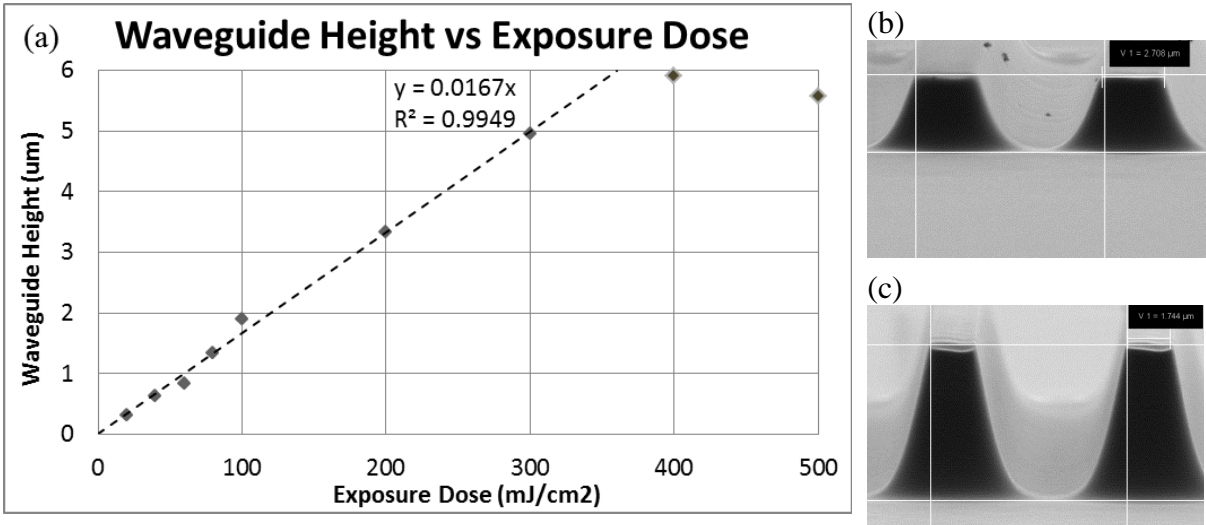


**Figure 4.2. Exposure ladder study of CYCLOTENE™ 6505**

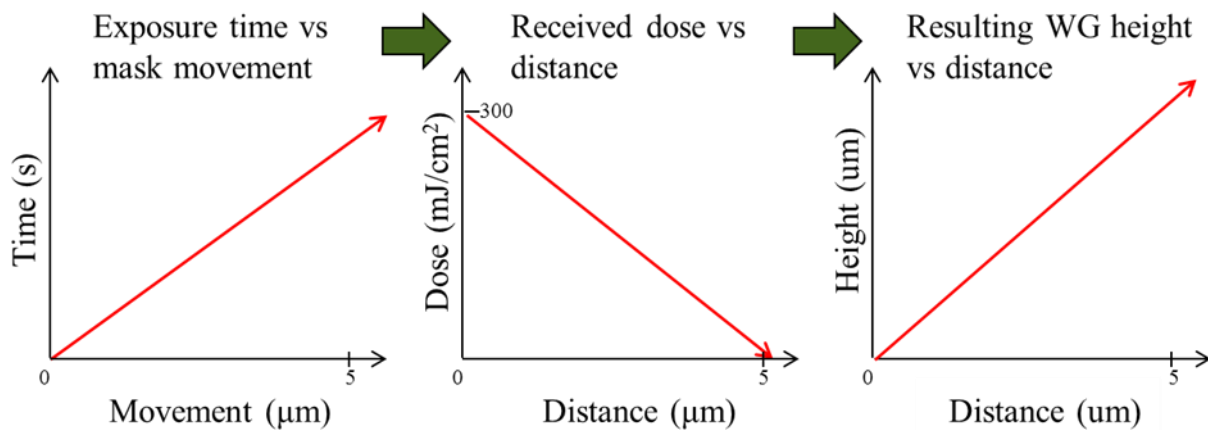
With the dose to height relationship established, precise input translation is implemented as illustrated in Figure 4.4. In practice, the moving mask method requires precise control of the exposure tool, in both the velocity of mask movement and the UV dosage. The UX-44101 mask aligner from Ushio turns out to be the ideal candidate to implement moving mask.

To adjust the angle of the end of the waveguide, the minimum dose needed for the waveguide height was calculated using Eq. 4.1, then the horizontal traveling distance required was calculated

by dividing the tangent of the angle to the waveguide height. Then the stage was programmed to move for the right amount of time to achieve a linear distribution of dose versus distance travelled.

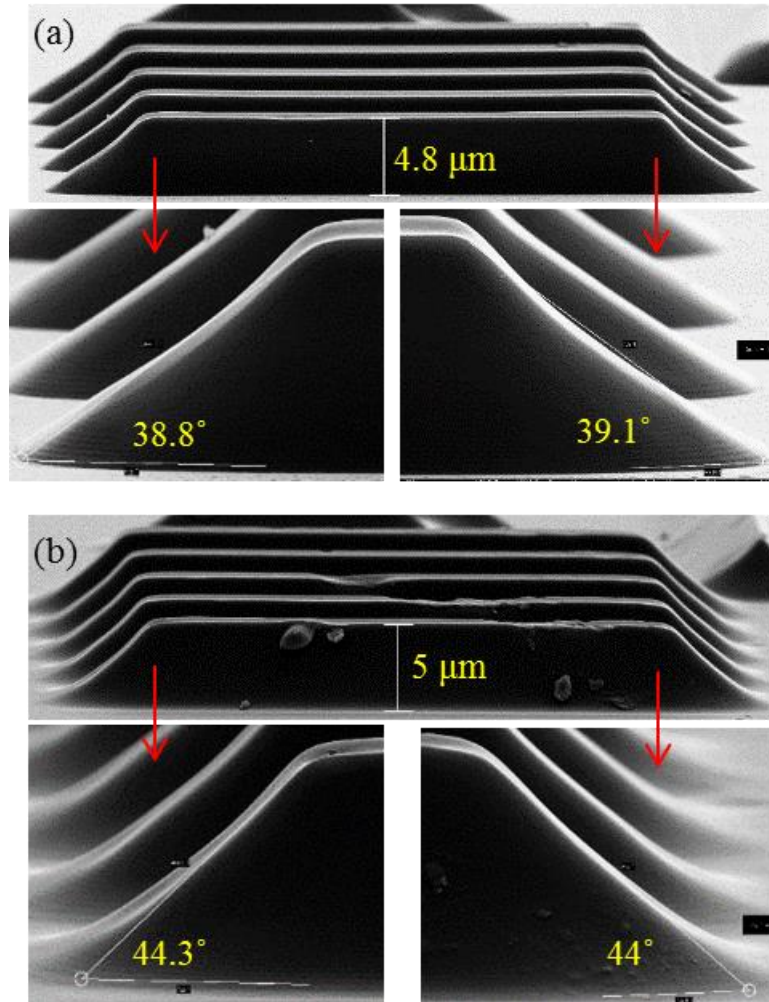


**Figure 4.3.** (a) Waveguide height versus exposure dose for the CYCLOTENE™ 6505 material, with two points highlighted: (b) height =  $3.4 \mu\text{m}$  at  $200 \text{ mJ}/\text{cm}^2$  dose and (c)  $5.87 \mu\text{m}$  at  $500 \text{ mJ}/\text{cm}^2$  dose



**Figure 4.4.** Translation of stage movement to received dose, then to the resulting waveguide sidewall angle

To achieve 40° entry and exit turning waveguides, an exposure with a dose ranging from zero to 350 mJ/cm<sup>2</sup> was performed over a translation distance of 6 μm. To achieve 45° entry and exit turning, an exposure with a dose of 400 mJ/cm<sup>2</sup> was performed over a translation distance of 6 μm. The results are shown in Figure 4.5.



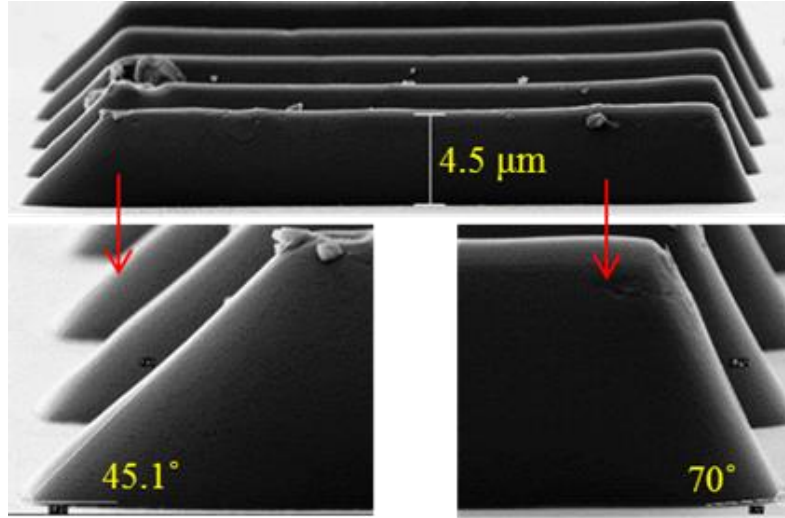
**Figure 4.5. Single mode waveguides with built-in TIR turning mirror by moving mask method with (a) 40 ° and (b) 45° turning angle**

The resulting oblique structures were measured to be 39° & 44° using SEM, which is consistently lower than the targeted angles of 40° & 45°. The consistently lower value is likely

due to miscalculation of the waveguide height after curing versus the stage movement. Since the waveguide height after curing can be controlled consistently, the stage movement can be adjusted accordingly to achieve the exact angles. The angle variation is found to be less than  $0.5^\circ$ . Smooth sidewalls were achieved through the slight reflow during curing and are helpful in ensuring low optical loss.

Two options are available to achieve the fiber coupling at the end faces as shown in Figure 4.1: (a) dicing followed by edge polishing or (b) a modification to the moving mask lithography. Dicing at waveguide edge introduces a practical challenge, as the waveguide edge must also be located at interposer edge, not allowing any alignment structure. On the other hand, a modified moving mask method is compatible with alignment grooves, and it does not require any additional process steps.

The modified moving mask lithography was implemented by adding a steady exposure after the completion of the moving exposure, thereby fully exposing one end of the waveguide structure. Initial results from the implementation of such a method are shown in Figure 4.6. While  $45^\circ$  facets were achieved on the turning end, the sidewall angle was not near  $90^\circ$  on the straight end, and measured close to  $70^\circ$ . This reduced sidewall angle is attributed to excess exposure dose, which cannot be eliminated in this process. As a result, coupling efficiency of TIR waveguides are limited by the sidewall angle at the fiber-waveguide end. More on this will be covered in the next section.

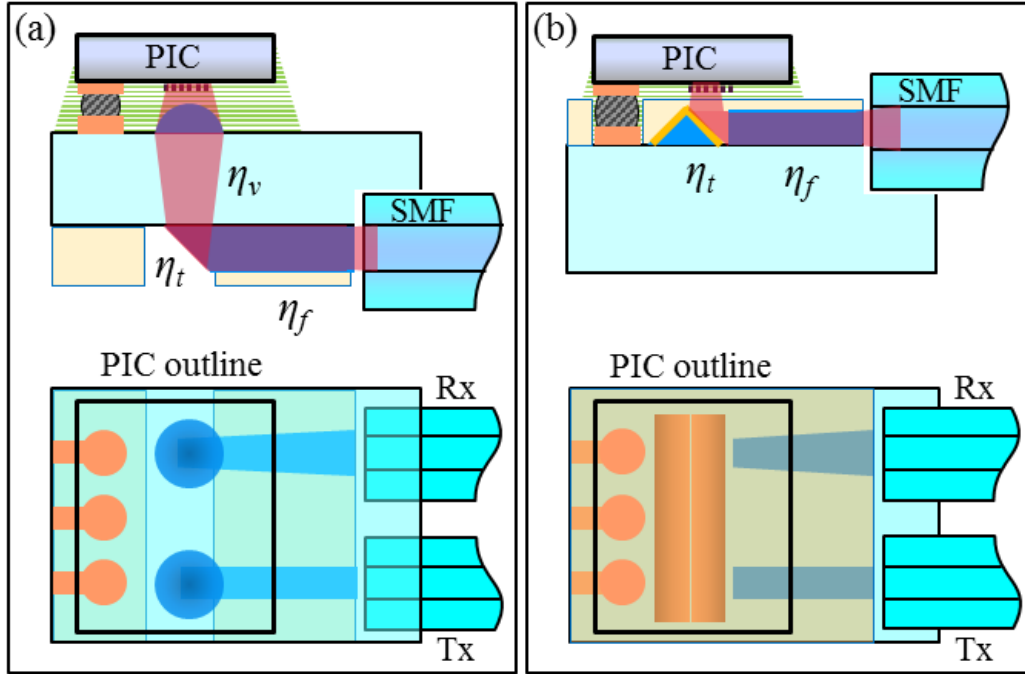


**Figure 4.6. One-sided turning single mode waveguides with 45° on the turning end and 70° on the straight end**

## 4.2 Modeling of Out-of-Plane Turning Structures

With the initial process development completed, the turning structures are carefully analyzed prior to design and fabrication. Extending from the Gaussian beam analysis presented in Chapter 3, the analytical model for the turning structures is shown in Figure 4.7.

The coupling efficiency and tolerance of the two designs were modeled using a combination of OptiFDTD and OptiBPM software. FDTD (Finite Difference Time Division) method was used to model the turning structures, while 3D BPM (Beam Propagation Method) was used for fiber alignment to planar waveguide. Two different types of simulation are used because the computationally intensive FDTD is not necessary for paraxial coupling from waveguide to fiber, where using FDTD will not gain additional information but will only burden computation resources.



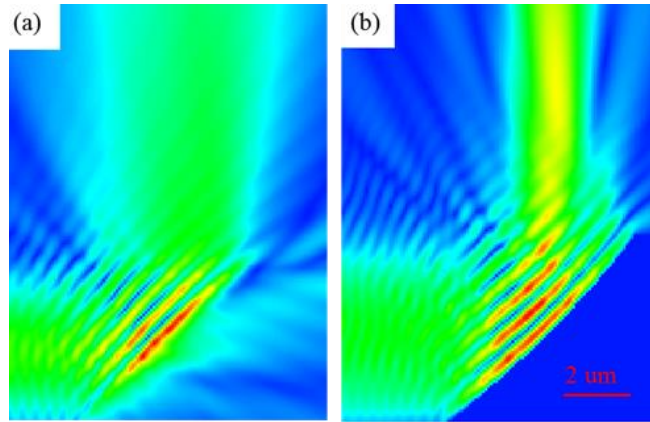
**Figure 4.7. Analytical model for (a) TIR turning and (b) Metallic turning structures in glass, coupling between planar aligned optical fiber and Photonic IC**

#### 4.2.1 FDTD Modeling of Turning Mirror

FDTD has been used to model single-mode photonics for 20 years. The theory of FDTD will not be covered in this thesis. Instead, interested readers are referred to the following two resources [64], [65]. 2D FDTD is ideal for modeling out-of-plane turning of single-mode transmission.

Similar to Chapter 3, a process aware model is constructed based on initial process development results shown in the previous section. Referring to Figure 4.5, it was noted that the sidewall achieved by moving mask method are consistently concaved due to reflowing of BCB. This concave shape may be helpful in focusing the light. To prove this concept, the concave sidewall is curve-fitted by an exponential tapering function with  $\alpha = 0.5$  in a 2D FDTD model with step size of 50 nm. The simulation results are shown in Figure 4.8. The turning loss at exactly  $45^\circ$  were 0.62 dB for TIR turning and 0.17 dB for metallic turning. Visible radiation loss can be observed at the

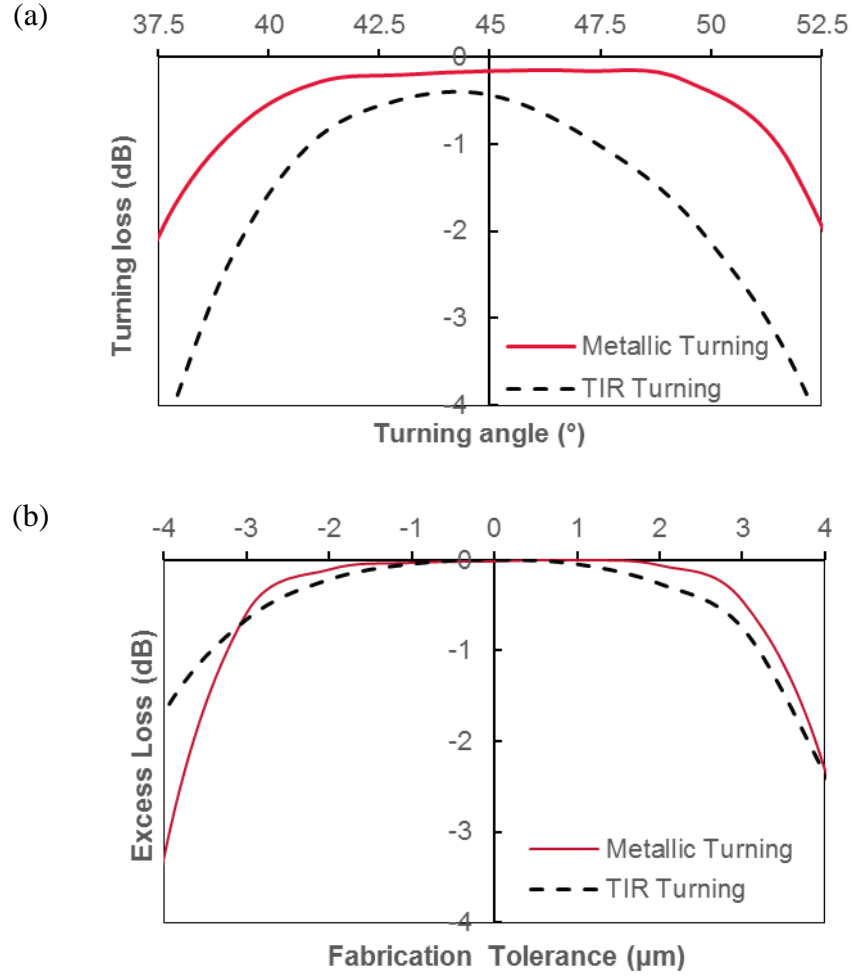
TIR turning interface, due to the concave sidewall. If the sidewall is straight, the simulation showed around 0.5 dB loss. On the other hand, the concaved shape helped focusing the light for metallic turning.



**Figure 4.8. 2D FDTD simulation results for (a) TIR and (b) metallic turning structures with accurately modeled sidewall profile based on process development results**

The modeled fabrication tolerance is shown in Figure 4.9. The 1-dB tolerance to turning angle variation is measured from the top of the model; it is  $\pm 3^\circ$  for TIR turning and greater than  $\pm 5^\circ$  for metallic turning. The alignment tolerance is 3  $\mu\text{m}$  for both cases, but for TIR turning it is the misalignment between the turning mirror and the lens on the other side of glass, while for metallic turning it is the misalignment between the turning mirror and the planar waveguide.

The TIR turning is inferior in all aspects, and is dropped from further consideration.



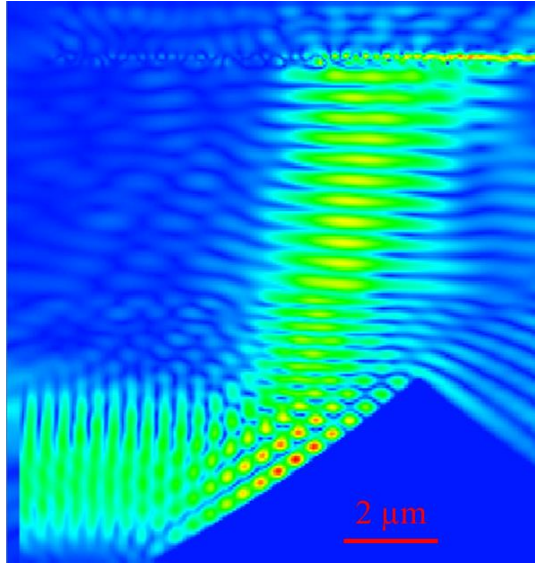
**Figure 4.9. Turning loss sensitivity with respect to (a) turning angle and (b) alignment for both metallic and TIR turning**

The simulation above was done without considering the vertical grating coupler interface at the die end. The angular tolerance numbers seems too optimistic. To get more realistic efficiency and tolerance numbers, a VGC based on literature is incorporated in the metallic turning model [66]. The input waveform is still located on the waveguide on glass, but now the output is measured from the silicon waveguide, after the out-of-plane turned light has passed through 10 μm of cladding and 20 μm of underfill materials. The resulting  $E_y$  field for the scenario with the lowest coupling loss, with the loss breakdown, is shown in Figure 4.10. Notice that to achieve highest



efficiency coupling to VGC, the out-of-plane turning needs to have a  $10^\circ$  offset, which equates to a turning angle of  $41^\circ$ . The coupling loss of VGC itself is the most significant contributor to overall loss, at 1.61 dB. This is consistent with literature. In fact, the impact of VGC is wide ranging, as the back reflection is likely the cause of additional loss in the other two interfaces.

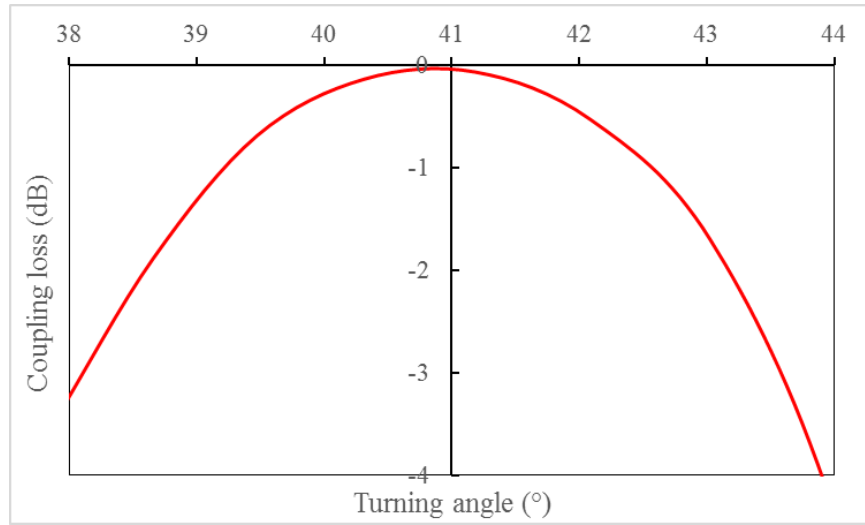
One of the key concerns with VGCs is the sensitivity of their coupling efficiency with respect to the wavelength. One of the key advantages of the metallic turning mirror presented in this thesis is its immunity to wavelength variation. Two additional FDTD modeling done in different wavelengths (1530 and 1570 nm) revealed that, while the VGC loss increases to around 2.2 dB, the rest of the loss remains under 0.9 dB. The slight increase is attributed to be caused by the VGC, meaning the turning mirror itself is relatively immune to wavelength difference.



Segment	Loss
Turning	0.37 dB
Mirror-to-VGC space	0.45 dB
VGC	1.61 dB
Total Loss	2.43 dB

**Figure 4.10. 2D FDTD modeling of out-of-plane turning structure coupling to a VGC based on literature, and the breakdown of coupling loss at optimum coupling**

The 1-dB angular tolerance is also modeled as shown in Figure 4.11, the tolerance is now only  $\pm 1.5^\circ$ .



**Figure 4.11. Angle tolerance of metallic turning taking into account of coupling to a VGC**

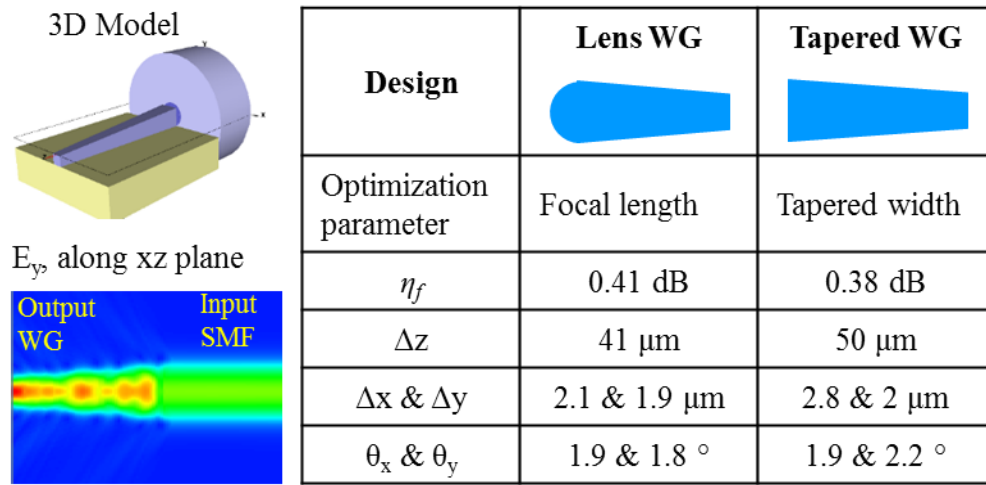
The analysis thus far has been 2D only, and for a good reason – 3D FDTD is very computationally intensive and if the structure is simply extruded along the remaining direction, 2D modeling would suffice [67]. However, in actual implementations curved VGCs have been developed to focus the beam in two axis [68]. A straight mirror will not be sufficient in focusing the axis coming out of the 2D plane. To address this, a curved mirror is designed as was shown in Figure 4.1.b. The curved mirror is designed to have a radius of curvature of  $10\ \mu\text{m}$  to focus the light beam for the  $20\ \mu\text{m}$  distance of travel. To accurately model this, 3D FDTD is required. Unfortunately, at the writing of this thesis the 3D modeling has yet been completed. However, the structure has been included in the design, and has already been fabricated and characterized.

#### 4.2.2 BPM Modeling of Fiber-to-Waveguide Coupling

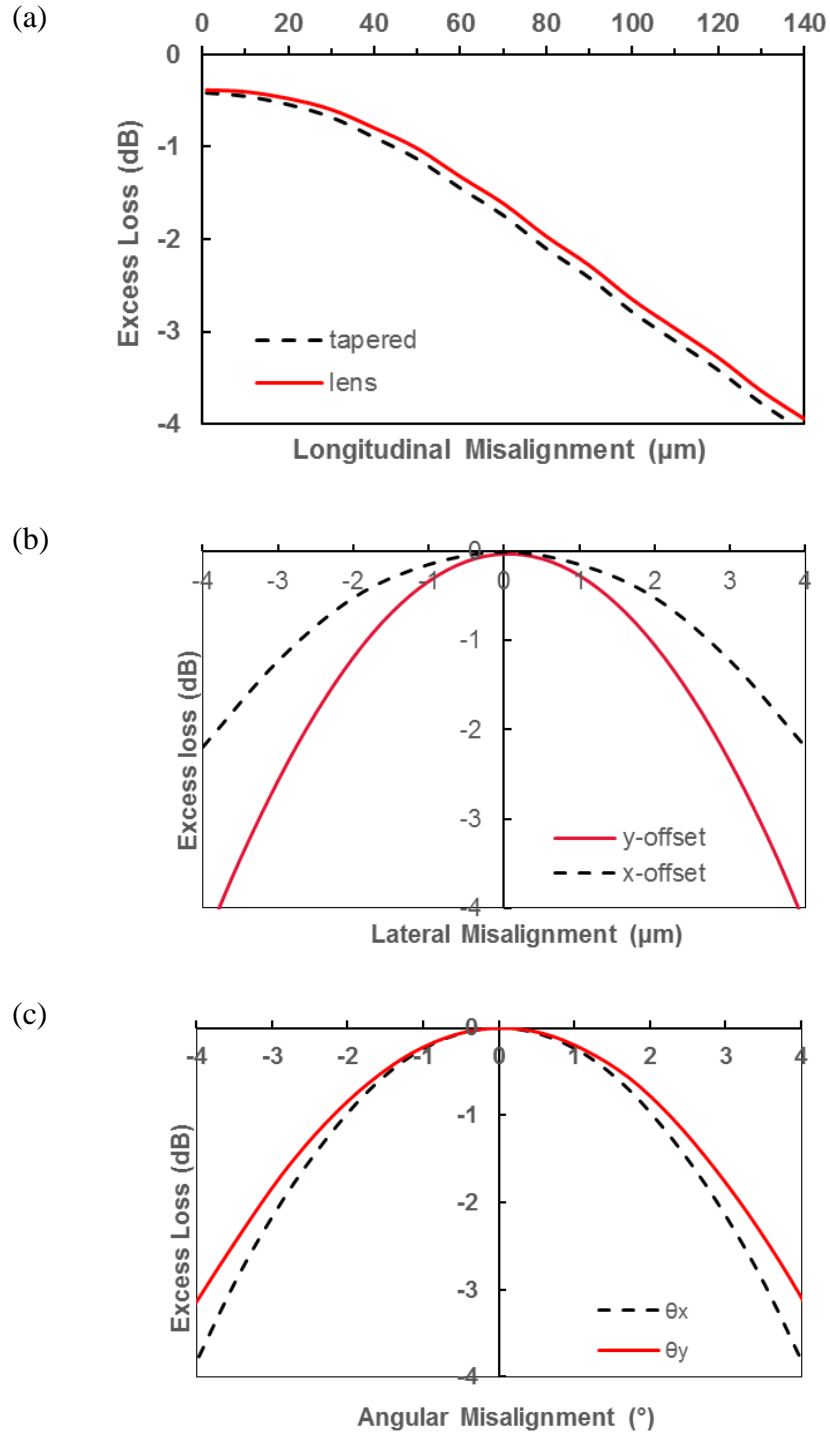
The coupling loss and misalignment tolerance of waveguide-to-fiber interface is modeled by 3D BPM. Two different types of waveguide end are considered: tapered to  $10\ \mu\text{m}$ , or lensed with

radius of curvature = 10  $\mu\text{m}$ . The model is summarized in Figure 4.12. At perfect alignment and 20  $\mu\text{m}$  gap, the simulated coupling loss is 0.4 dB, which is due to the distance (0.15 dB) and the mode mismatch (6.5  $\mu\text{m}$  comparing to 8.2  $\mu\text{m}$  in a standard SMF). The 1-dB tolerance is found to be 2.5  $\mu\text{m}$  in the x direction and 2  $\mu\text{m}$  in the y direction. The x-direction tolerance is on par with fiber-to-fiber coupling due to the tapered waveguide design, whereas the y-direction tolerance is limited by the achievable thickness of the optical waveguide. Similar modeling is done with respect to the tilt, where the 1-dB tolerance is found to be around  $2^\circ$ . The z-direction 1-dB tolerance is 40  $\mu\text{m}$ . The tolerance results are shown in Figure 4.13.

The lensed waveguide is worse in all aspects, and is dropped from further consideration.

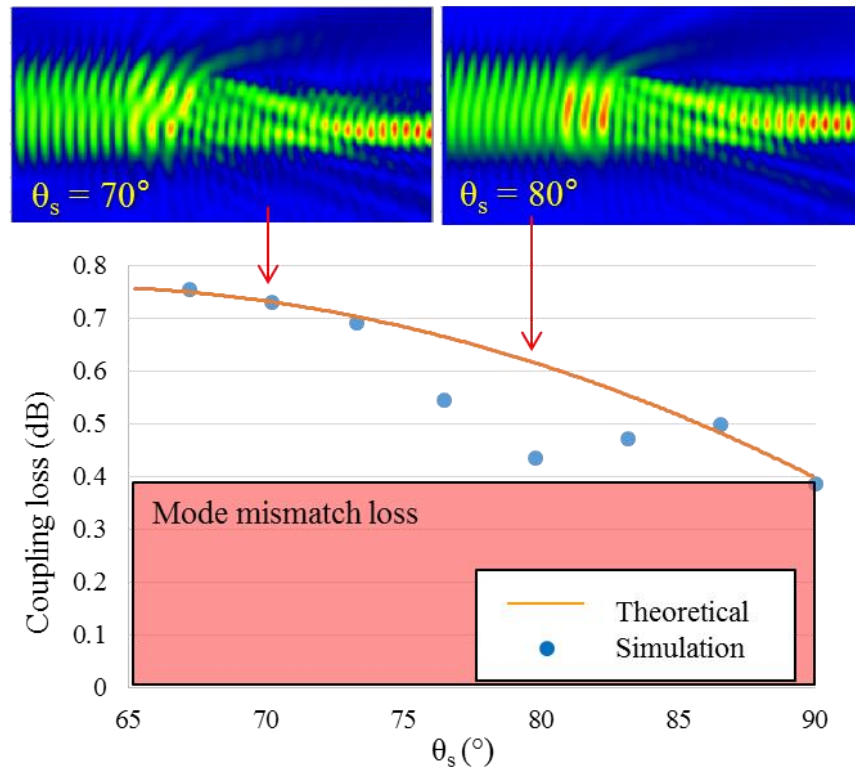


**Figure 4.12. 3D BPM modeling of fiber-to-waveguide coupling, showing coupling efficiency and 1-dB tolerance numbers. Tapered waveguide is superior in all regards**



**Figure 4.13. 1-dB misalignment tolerance in (a) z direction, (b) x and y directions, and (c) angular tilt along the x and y axis**

Recall, in Chapter 3, that the waveguide sidewall is not 90 degrees for the 6505 BCB material. A BPM model is constructed to analyze coupling efficiency as a function of the sidewall angle at the end facet, as shown in Figure 4.14. As the sidewall angle decreases, one would expect the coupling efficiency to go down proportionally, similar to angular misalignment investigated in previous page. Surprisingly, the simulated efficiency at  $80^\circ$  is close to the peak efficiency, 0.38 dB, at  $90^\circ$ . The reason for the enhanced efficiency is due to the serendipitous combination of the larger core area due to the tile, and the small enough tilt angle. Once the sidewall angle is below  $80^\circ$ , the effect of larger core area is no longer significant enough, and the efficiency follows that of typical angle tilt.



**Figure 4.14. 3D BPM simulation of fiber to waveguide coupling loss with respect to sidewall angle of waveguide**

For waveguides fabricated for TIR turning mirror using modified moving mask lithography, the measured sidewall is  $70^\circ$ , which will add 0.3 dB of additional coupling loss. On the other hand, planar fabricated waveguides used for metallic turning mirror, with  $80^\circ$  sidewall, can achieve optimum coupling. All things considered, the combination of curved metallic turning with straight tapered waveguide can achieve the lowest coupling loss and the most relaxed fiber alignment tolerance with just a few added process steps. This will be the default structure going forward, and its properties are listed in Table 4.1.

**Table 4.1. Summary of Optimized Turning and Coupling Structures**

<b>Turning Mirror</b>	<b>Metallic</b>
Min coupling loss (by itself)	0.17 dB
Min coupling loss (w/ VGC)	0.82 dB (discounting VGC loss)
Angle sensitivity	$\pm 1.5^\circ$ @ 1 dB
WG to turning sensitivity	$\pm 3\mu\text{m}$ @ 1 dB
WG sidewall	$80^\circ$
Process steps	Moving mask turning, mirror coating, patterning, planar waveguide fabrication, applying cladding
Process requirement	Turning-to-WG alignment  < $3\mu\text{m}$
<b>Fiber-WG</b>	<b>Tapered</b>
Min coupling loss	0.38 dB
x & y tolerance	$2.8\mu\text{m}$ & $2\mu\text{m}$ @ 1 dB
$\theta_x$ & $\theta_y$ tolerance	$2.2^\circ$ & $1.9^\circ$ @ 1 dB
z tolerance	$50\mu\text{m}$ @ 1 dB

### 4.3 Design of Out-of-Plane Turning Structures

The design incorporates four different types of structures:

**1) Process monitor:** These structures contain short waveguide arrays, straight and curved mirrors, and lens arrays. Specifically, it contains waveguide arrays at 10, 7, and 5  $\mu\text{m}$  line and space by themselves and intercepting to turning mirrors. The curved mirrors have a radius of curvature correlating to its width, at 10, 7, and 7  $\mu\text{m}$  respectively. The lens arrays have diameter and spacing of 20, 15, and 10  $\mu\text{m}$ . In addition, there's a cross for quick visual reference.

**2) Fiber coupling:** Four waveguides at 250  $\mu\text{m}$  pitch, with semicircular alignment structures on top of turning mirror. The other end is terminated flat for fiber coupling. Both straight and tapered (to 10  $\mu\text{m}$ ) waveguide ends are available.

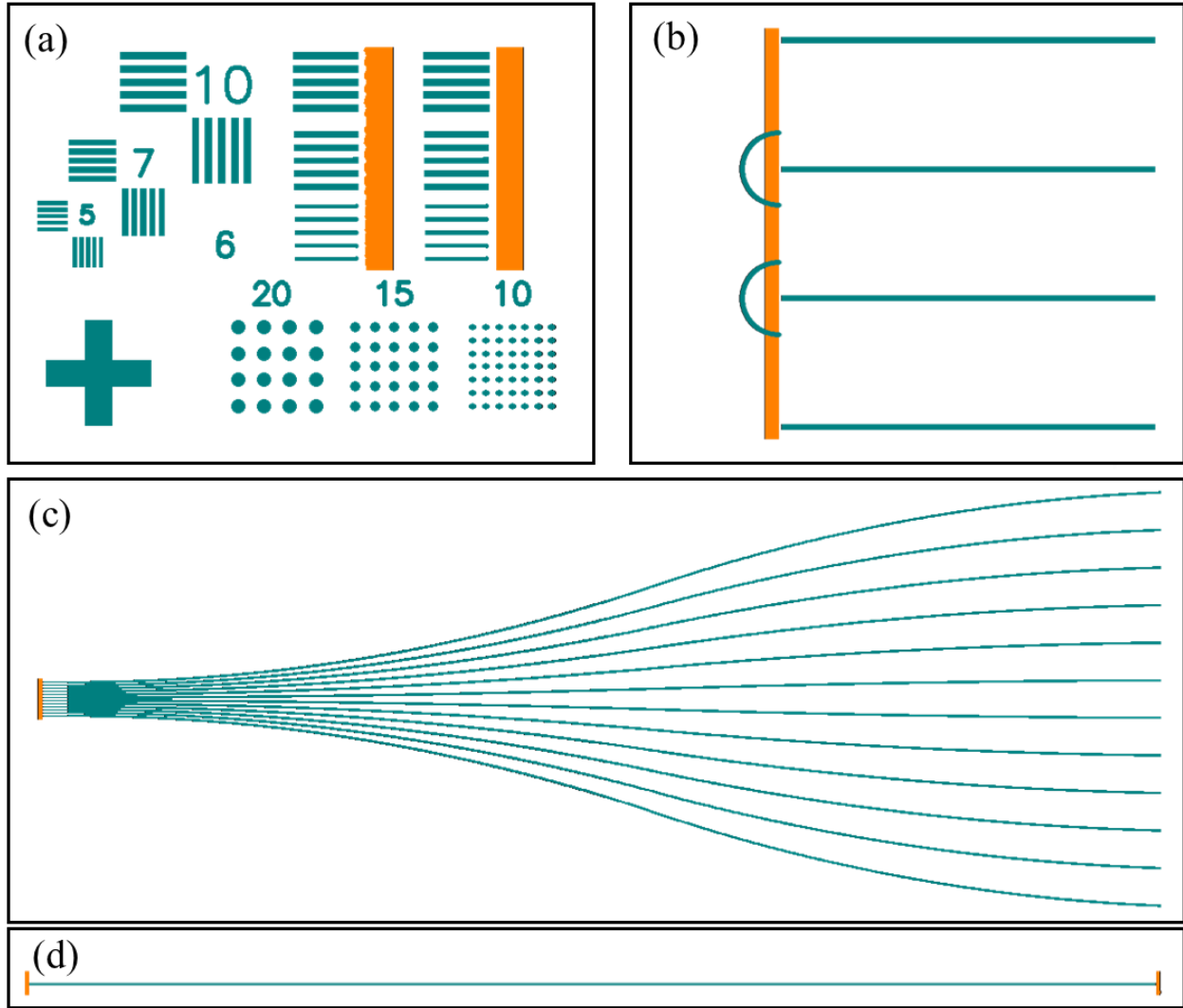
**3) 12x1 fan-in:** 12 waveguides at 250  $\mu\text{m}$  pitch, then fan-in to 20  $\mu\text{m}$  pitch, with both straight and curved turning mirrors at the 20  $\mu\text{m}$  pitch end.

**4) Single line:** Single waveguide with turning mirrors on both ends, both short and long lines are available. Short lines are for visual reference. Both straight and tapered (to 10  $\mu\text{m}$ ) waveguide ends are available.

Snapshots of the test structures are shown in Figure 4.15.



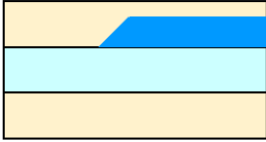
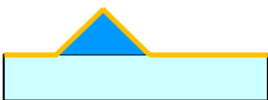
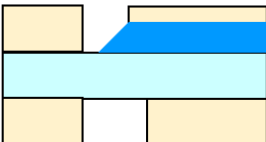
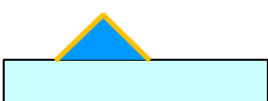
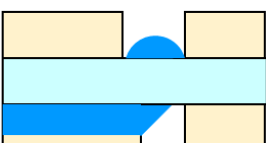
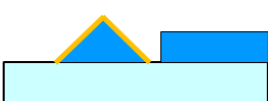
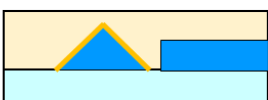
### 4.4 Fabrication of Out-of-Plane Turning Structures

The fabrication process for TIR turning and metallic turning structures are shown in Figure 4.16. In either process, the first step is moving mask lithography. Moving mask lithography utilizes the same process as described in Table 3.1, except for the lithography, which is detailed in Table 4.2. To minimize effects of stage acceleration and deceleration, the shutter opening is programming during the middle of stage movement.



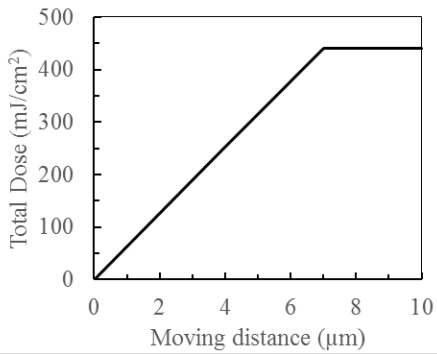
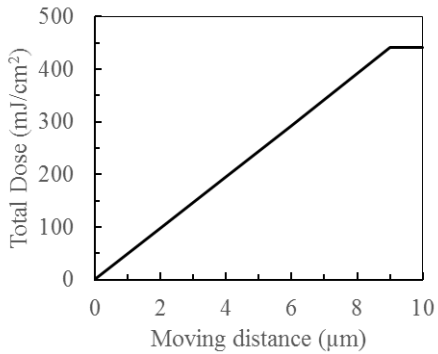
**Figure 4.15. Layout view of the out-of-plane turning test structures, not to scale, showing (a) process monitor, (b) fiber coupler at 250  $\mu\text{m}$  pitch, (c) fan out coupler, and (d) single line. Orange color indicates turning mirror, while blue color indicates planar waveguide**



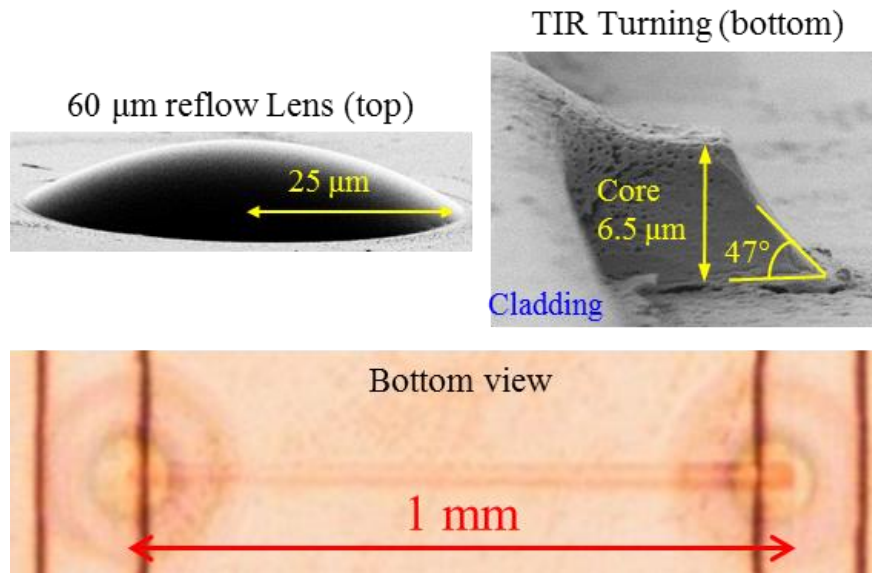
TIR Turning	Process	Metallic Turning	Process
	Turning WG by moving mask		Turning mirror by moving mask
	Apply cladding on both sides		Ti-Cu sputtering
	Cladding opening by photolithography		Mirror formation by etching
	Flip over, lens formation by reflow		WG formation
			Apply top cladding

**Figure 4.16. Process flow for out-of-plane turning structures on glass**

**Table 4.2. Moving Mask Lithography Process**

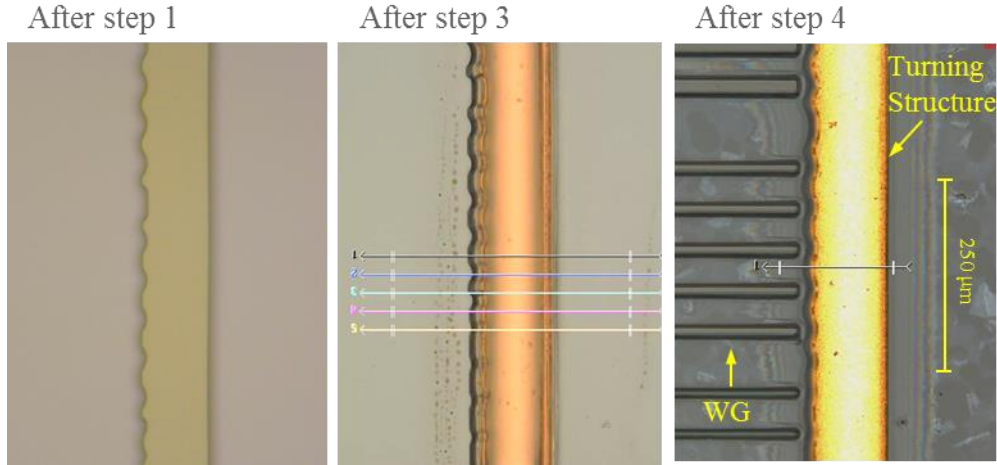
Angle needed	45°	41°
Stage movement speed	10 $\mu\text{m/s}$	
Exposure power	365 nm, 70 $\text{mJ/cm}^2/\text{s}$	
Shutter open time	0.7 s	0.9 s
Repeat time	9 times	7 times
Resulting exposure dose vs distance		

The short line structure is used to assess the quality of TIR turning, as shown in Figure 4.17. One glaring process challenge is apparent with the process flow proposed – the cladding opening is unprotected after fabrication, which means the TIR turning surface is susceptible to contamination during the rest of the process steps. The same can be said about the lens. In all, the TIR turning process presents more potential challenges than initially expected.



**Figure 4.17. TIR turning structure fabricated using the process flow developed in this thesis, showing the lens on top and the turning structure on the bottom**

The process monitor structure is used to assess the quality for the metallic turning structures. The snap shot of process monitor after each step of process is shown in Figure 4.18. Unlike the TIR process, the turning structures are “protected” by a sputtered titanium-copper reflective layer right after curing, and will be sealed off from contamination after application of cladding layer. Therefore, the quality of the turning mirror can be maintained. In addition, the planar processed waveguide can have a straighter sidewall.



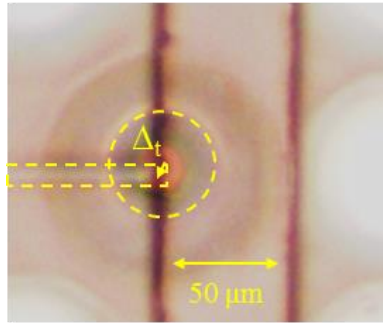
**Figure 4.18. Process monitor of metallic turning structure**

The fabrication tolerance for both TIR turning and metallic turning structures are measured based on fabricated samples across a glass panel. The results are summarized in Figure 4.19. As shown, the misalignment of lens to waveguide across the glass is greater than  $3\text{ }\mu\text{m}$ , failing to meet the 1-dB tolerance calculated in the previous section.

On the other hand, because the alignment between the metallic turning and the waveguide is planar on the same side of glass, the process variation is less than  $2\text{ }\mu\text{m}$ , within the 1-dB tolerance calculated in the previous section.

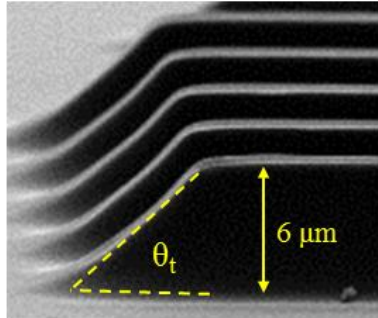
The angular variation is remarkably low across the glass panel, at less than  $1.3^\circ$ . Recall the 1 dB tolerance is  $1.5^\circ$ , which means the moving mask process can indeed produce repeatable turning structures at high throughput within tolerance.

To summarize, the metallic turning structure has met both 1-dB alignment tolerance requirement calculated earlier in this Chapter. The optical loss of such a turning structure is covered next.



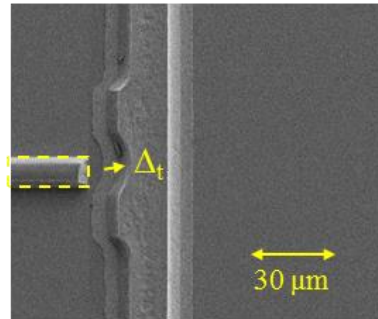
$\Delta_t :=$  turning to lens offset  
 Lens to waveguide alignment is **indirect** using electrical vias as reference

$\Delta_{t\_avg}$	3.8 $\mu\text{m}$
Std. Dev	2.82 $\mu\text{m}$



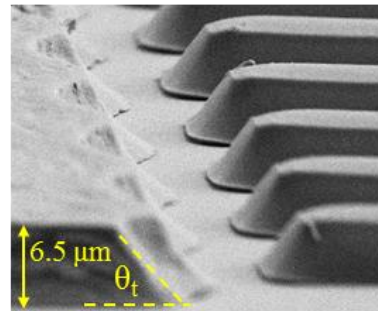
$\theta_t :=$  Turning angle offset  
 Sidewall shape detrimental

$\theta_{t\_avg}$	44.3°
Std. Dev	1.3°
Sidewall	Scattering



$\Delta_t :=$  turning to WG offset  
 Direct WG alignment to turning mirror

$\Delta_{t\_avg}$	1.625 $\mu\text{m}$
Std. Dev	0.54 $\mu\text{m}$



$\theta_t :=$  Turning angle offset  
 Sidewall shape beneficial

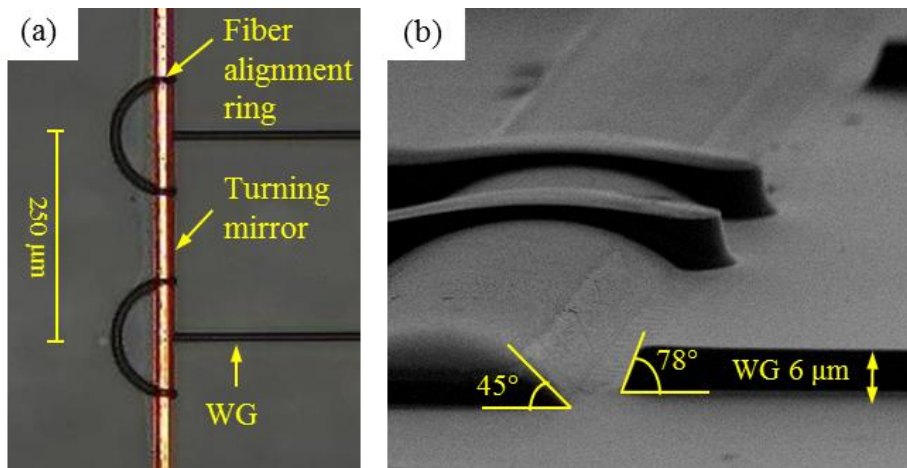
$\theta_{t\_avg}$	45.9°
Std. Dev	0.8°
Sidewall	Focusing

**Figure 4.19. Fabrication tolerance study for both TIR turning structure and metallic turning structure**

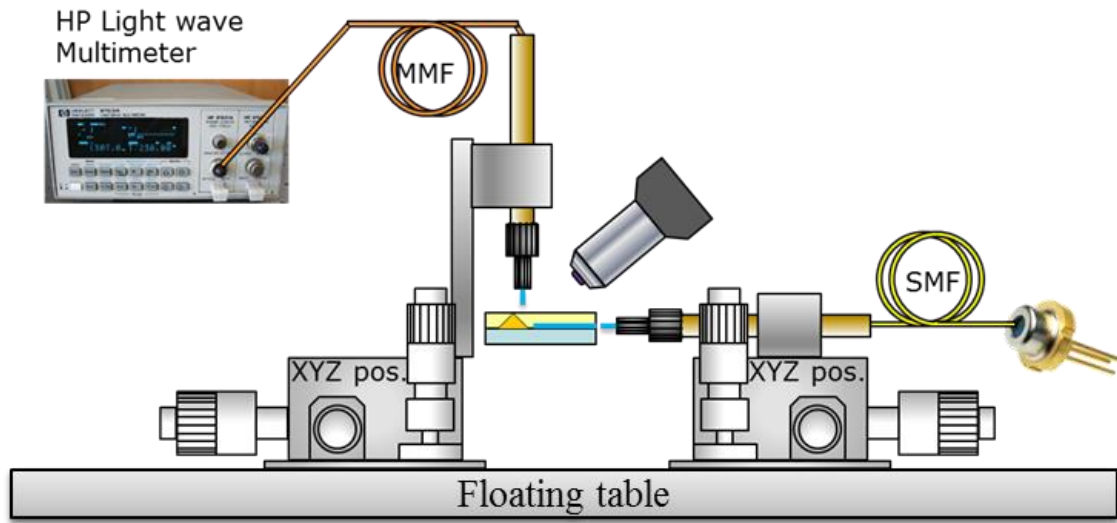
#### 4.5 Characterization of Out-of-Plane Turning Structures

Optical loss measurement is performed on the metallic turning structure as shown in Figure 4.20. As shown in the figure, a “fiber alignment ring” is designed on the same mask as the planar waveguides to help with visual alignment during measurement. The testing setup is shown in Figure 4.21. The setup is similar to the one used in Chapter 3 to measure the planar waveguides.

The turning loss is calculated based on measuring the total loss, then subtracting the waveguide-only loss measured in Chapter 3. For a 2 cm long waveguide, the waveguide-only loss is estimated by adding the fiber-to-waveguide coupling loss and the waveguide propagation loss. For completeness, the loss is measured for three different wavelengths, even though the waveguide is not single-mode at lower wavelengths. The optical loss measurement results are shown in Table 4.3. The measured turning loss is greater than 1.5 dB, whereas the simulated value is less than 1 dB. Further separation of loss components is difficult with existing setup in the characterization lab; therefore, possible sources to the excess optical loss are listed here: the surface roughness of the metallic turning, the shape of the turning arc, and the true reflectivity of copper coating.



**Figure 4.20. Fiber coupling structure with fiber alignment ring and turning mirror**



**Figure 4.21. Characterization setup for metallic mirror turning loss**

**Table 4.3. Characterization results, with coupling and propagation loss through waveguide removed based on measurement results from in Chapter 3**

Wavelength	Loss (dB)	WG only loss (dB)	Turning loss (dB)
850 nm	3.34	2.29	1.05
1310 nm	5.06	3.17	1.89
1550 nm	5.03	3.34	1.69

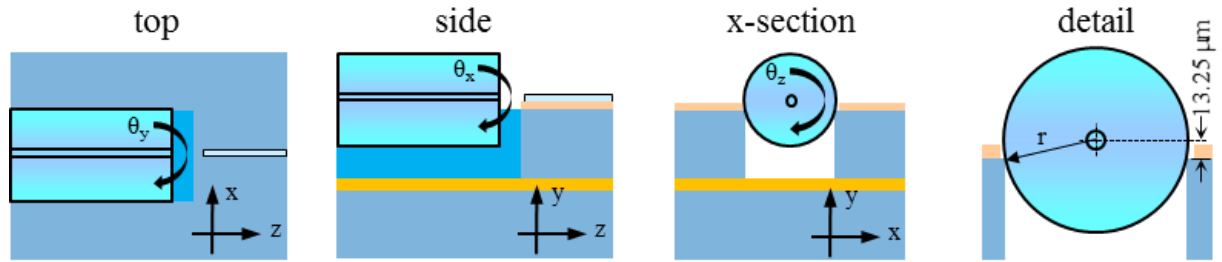
#### 4.6 Fiber Alignment Grooves

Passive alignment of optical fibers can be achieved mechanically using precisely manufactured structures on the substrate such as v-grooves, which can be fabricated at 54.7° sidewall using anisotropic wet etching on silicon along its crystalline plane. Unfortunately, glass is amorphous and does not lend itself to precision wet etching with a controllable sidewall angle. Dry reactive

ion etching (DRIE) of glass cavities have been attempted and showed capability of achieving precise cavities, but the reported etch rate is slow and energy intensive [69]. In this thesis, two mechanically diced u-groove structures in glass are proposed and explored.

#### 4.6.1 Two-Point Contact U-Groove

U-grooves fabricated using DRIE in silicon have been used for passive fiber alignment [70]. In this design, the width of the groove was assumed to be exactly the width of the fiber to restrict the misalignment in x-direction; however, nothing was done in the y-direction. To also establish a reference in the y-direction, a two-point contact u-groove design in glass, inspired by the reported work, is proposed as shown in Figure 4.22.

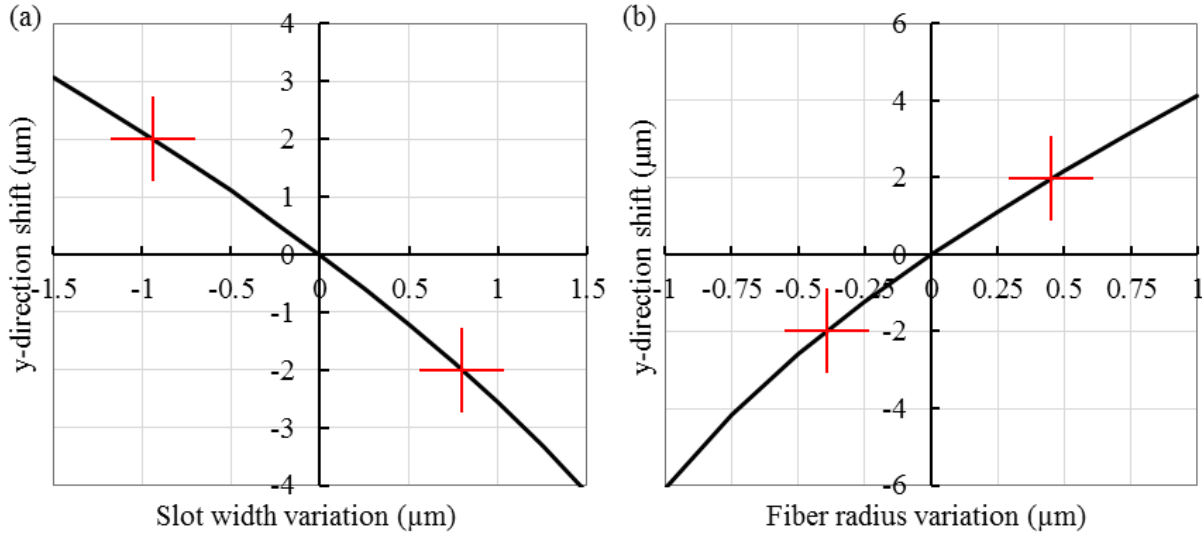


**Figure 4.22. The two-point contact u-groove design**

The u-shape is formed in glass by bonding two thin glass panels together, where one contains mechanically diced slots. Since it is difficult to handle and dice thin glasses less than 70  $\mu\text{m}$  in thickness, it was decided that the y-direction reference would not be established by the thickness of glass, but rather by precise width of the slot. Assuming 13.25  $\mu\text{m}$  offset is needed to align the fiber core to the waveguide core (10  $\mu\text{m}$  for dry film under cladding, and 3.25  $\mu\text{m}$  for half the height of waveguide core), the slot width needed is therefore

$$w_s = 2\sqrt{r^2 - 13.25^2} = 122.16 \mu m. \quad (4.2)$$

From the equation above, the y-direction misalignment sensitivity to variation in slot width and fiber radius is plotted in Figure 4.23. The y-direction 1-dB tolerance, from Table 4.1, is 2  $\mu m$ , which translates to the slot width and fiber radius variation limit of  $\pm 0.8 \mu m$  and  $\pm 0.39 \mu m$ , respectively. Since variations in fiber diameter is  $\pm 0.7 \mu m$  according to datasheet from Corning Inc., less than 0.5  $\mu m$  of margin was left for slot width variation. As a result, the two-point contact design was not pursued further beyond the initial trial, which is reported next.

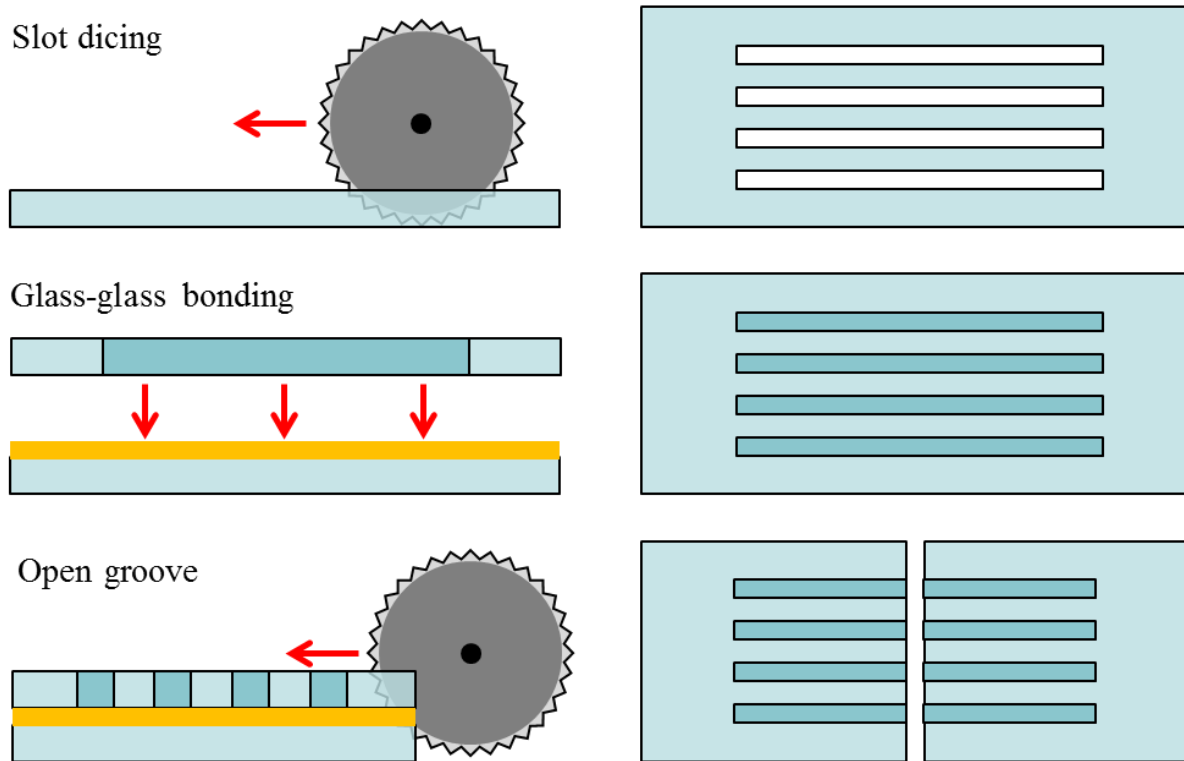


**Figure 4.23. The sensitivity of y-directional alignment to (a) slot width and (b) fiber radius variation for the two-point contact u-groove design**

The two-point contact u-grooves were fabricated on glass using the process flow as illustrated in Figure 4.24. The dicing was performed by DISCO Corporation. The material used for glass – glass bonding is called EPR-129, and it is provided by MicroChem Corporation. EPR-129 a



developmental material similar to the commercially available PermiNex™ 1000 [71]. The optimized bonding condition is listed in Table 4.4.



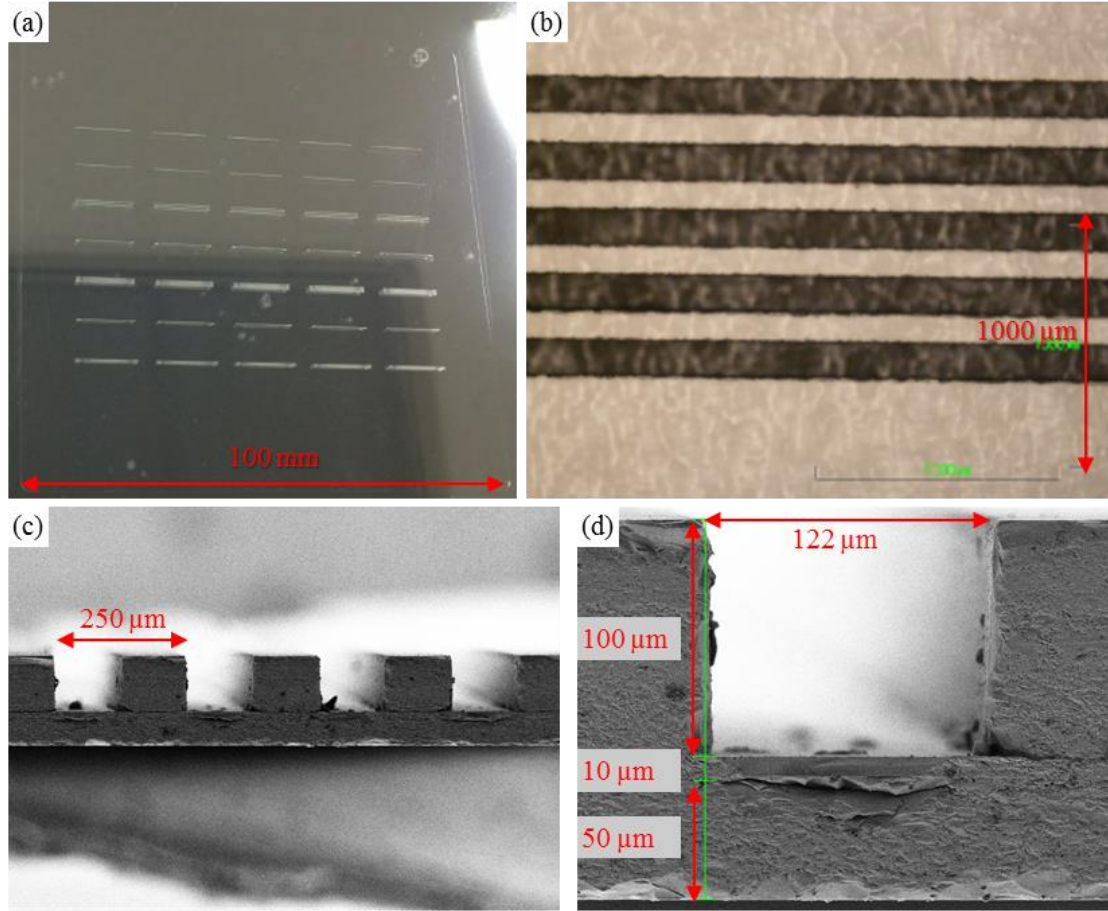
**Figure 4.24. Fabrication process flow for two-point contact u-grooves**

Typically, wafer bonding is performed by a dedicated bonder. Unfortunately, the square shaped glass panels are not compatible with wafer bonders. Instead, a planarizer tool provided by Brewer Science was used to perform glass-glass bonding. Similar to a wafer bonder, the Brewer planarizer bows the two sides before contact, thus minimizing formation of trapped bubbles.

**Table 4.4 Optimized glass – glass bonding condition with EPR-129**

<b>Process</b>	<b>Step</b>	<b>Condition</b>
Glass Substrate Cleaning	Plasma Clean	Plasma cleaner, O <sub>2</sub> , RF power 100 W, 100 C, 10 min
	Solvent Clean	Acetone, Methanol, IPA, DI water rinse, N <sub>2</sub> dry
	Drying	Hot plate, 100 C, 2 min
Bonding Material Application on bottom glass	Dispense EPR-129	Spin coater, 3000 RPM, 45 s
	Soft Bake	Hot plate, 95 C, 5 min
	Lithography	i-line, 1000 mJ/cm <sup>2</sup>
	Post-exposure bake	Hot plate, 7 C, 120 s
	Development	Not needed
Bonding & Curing	Bonding – placing slotted glass on top	Brewer Science planarizer, 150 C, 0.6 MPa, 30 s
	Thermal Cure	180 C, 60 min

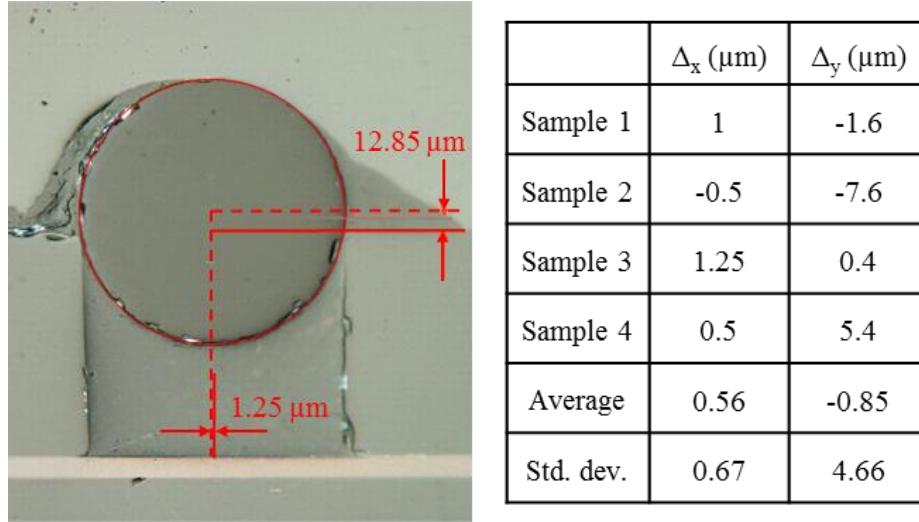
The fabrication results are summarized in Figure 4.25. The initial result showed no cracking after dicing for 100 and 150  $\mu\text{m}$  thick Corning glass. The same dicing pattern was also attempted on 50  $\mu\text{m}$  Schott glass, which cracked along every slot. At this point, it was not clear if the cracking was purely a function of glass thickness or also due to different glass compositions (Corning versus Schott). Regardless, 50  $\mu\text{m}$  glass was unusable.



**Figure 4.25. (a) A 100 mm<sup>2</sup> 100 μm thick glass panel with slots, (b) top view of one array of slots, (c) SEM view of a bonded and opened u-groove at 250 μm pitch, and (d) close-up view of one groove with 122 μm width at top**

The measured slot width at the top is 122 μm with a standard deviation of  $\pm 1$  μm, which exceeded the 1-dB alignment tolerance.

Fiber assembly trial was performed on five samples. One of the fibers was not secured properly during curing and was discarded. The assembly result of the four samples were summarized in Figure 4.26. The average  $\Delta_x$  and its standard deviation are both under 1 μm, within the 1-dB misalignment range.

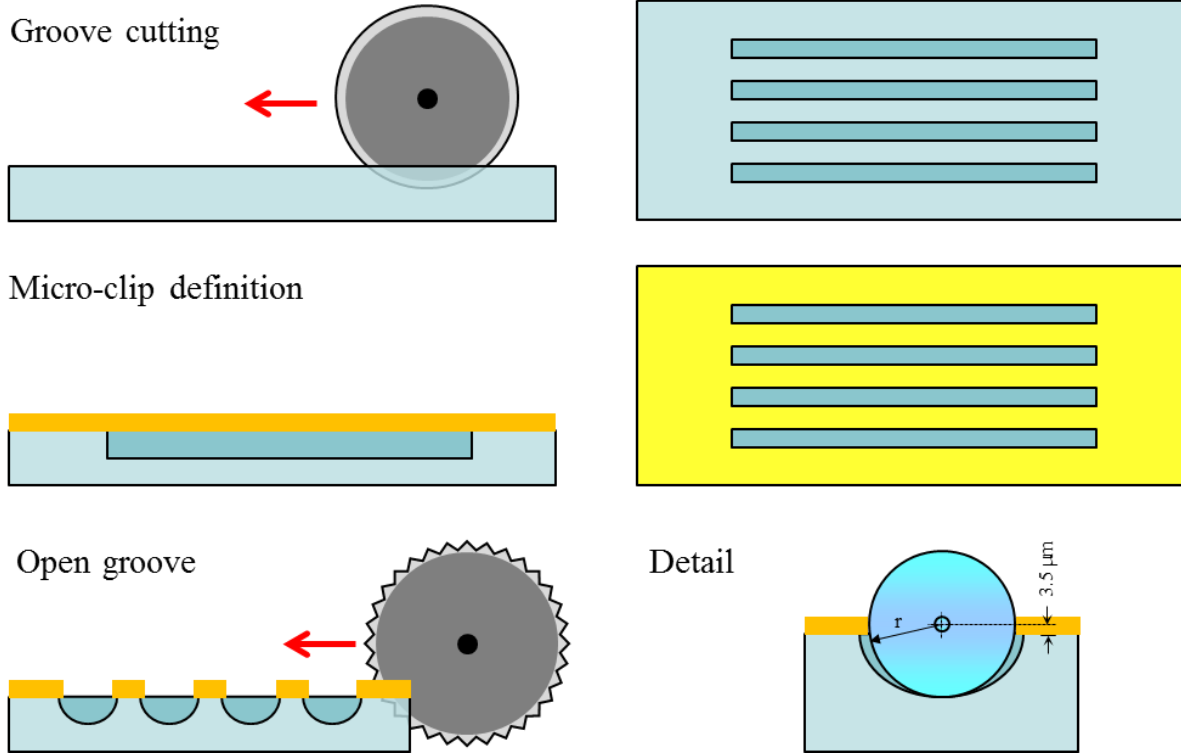


**Figure 4.26. Summary of fiber assembly trials performed on two-point contact u-grooves**

While the average  $\Delta_y$  is within the limit for the small sample size studied, the standard deviation implies the data varies widely. As analyzed previously, the weakness of the two-point contact u-groove is the y-directional sensitivity to variation in both fiber diameter and slot width. The result, consistent with the analysis, confirmed the limited application of this design. A new design – the shallow cut u-groove, was proposed to address the y-directional sensitivity.

#### 4.6.2 Shallow Cut U-Groove

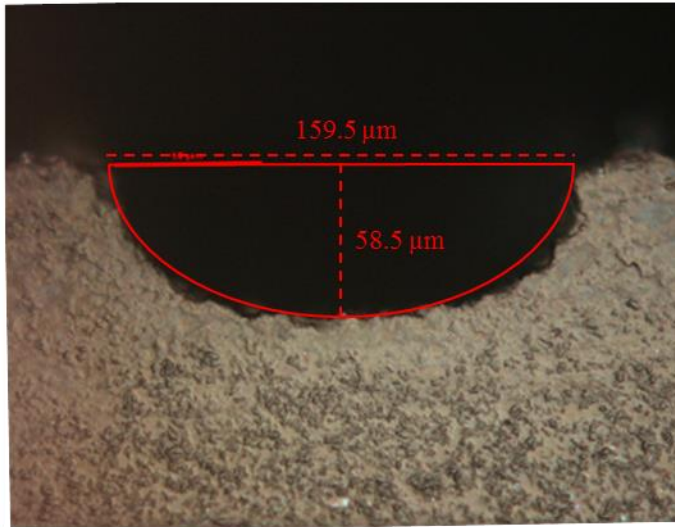
According to DISCO Corporation, the rounded dicing blades can achieve shallow grooves at 1  $\mu\text{m}$  level precision in depth (y-direction) without breaking the glass. The x-direction, however, cannot be easily defined by the shallow cut due to the rounded blade edges. To establish x reference, polymer micro-clips consisting of dry-film CYCLOTENE™ material was proposed, with process flow as shown in Figure 4.27. The application of the dry-film material is the same as documented in Table 3.2. Also shown in the figure is a detailed view fiber alignment, with x-direction alignment by polymer micro-clips and y-direction alignment by groove depth.



**Figure 4.27. Fabrication process flow and alignment scheme for shallow cut u-grooves**

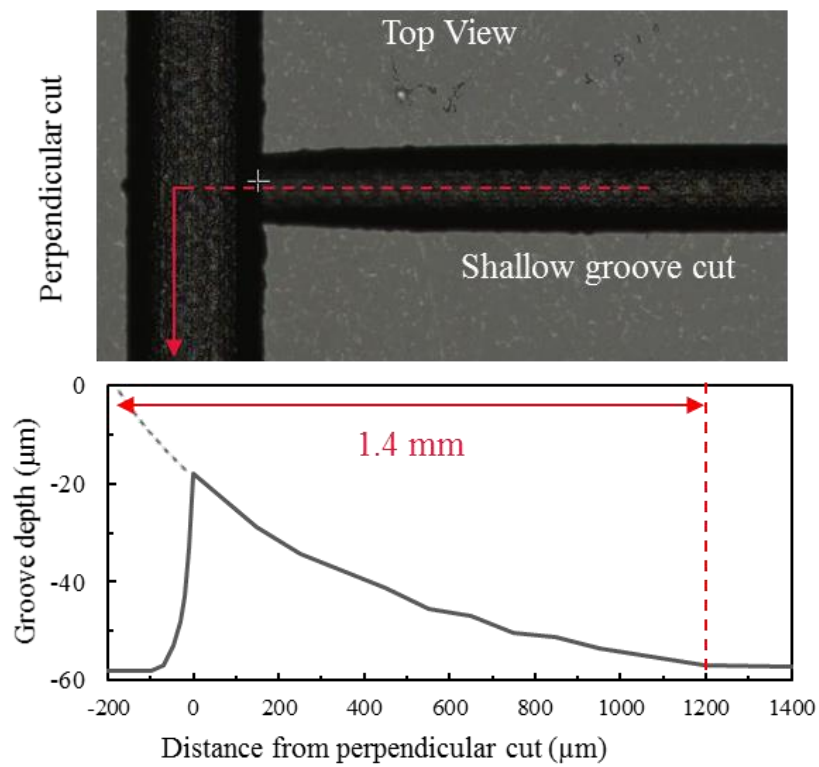
A series of shallow cuts were performed to test out the groove depth at the center, with the results summarized in Figure 4.28. While fairly consistent depth can be achieved with  $\Delta_y < 1 \mu\text{m}$  at the center of the groove, the groove depth is not constant along the edge of the groove due to the curvature of the blade. This curved edge will affect  $\Delta_z$ , as the fiber end sitting on the curved edge cannot abut to the waveguide end. A perpendicular cut along the edge of the groove might be able to overcome the edge effect; however, the curved region along the edge extends 1.4 mm long, as measured in Figure 4.29. 1.4 mm is more than 10 times the diameter of the fiber, which will require a perpendicular cut large enough for the fiber to easily bend and misalign. Therefore, the shallow cut groove design is unusable because it cannot simultaneously establish  $\Delta_y$  and  $\Delta_z$ .

No further fiber alignment groove designs were attempted for this thesis. Ideas for an improved design are included as “future works” in Chapter 6.



	Width (μm)	Depth (μm)
Sample 1	159.5	58.5
Sample 2	161	59.5
Sample 3	157	58
Sample 4	156	59.5
Sample 5	157	57.5
Sample 6	153.5	57.5
Sample 7	153.5	59.5
Sample 8	155.5	58.5
Average	156.6	58.6
Std. dev.	2.47	0.81

**Figure 4.28. Summary of shallow cut u-groove dimension at the center of the groove**



**Figure 4.29. Shallow groove edge as defined by the curvature of the blade**

## 4.7 Summary

Polymer-based out-of-plane turning structures fabricated using moving mask lithography have been studied in this chapter. Although other methods for fabricating turning structures have been explored in the past, none can address the throughput and quality requirements for high volume manufacturing. Moving mask lithography can achieve both by moving the entire mask during exposure, thus enabling turning structures to be made along the entire mask, with the same quality pending spin coat uniformity. Further, tailorable turning angle can be achieved by moving mask lithography by adjusting the shutter opening time and movement distance of the stage. Using moving mask lithography, turning mirrors at both  $41^\circ$  and  $45^\circ$  have been realized within  $1^\circ$  across a glass panel.

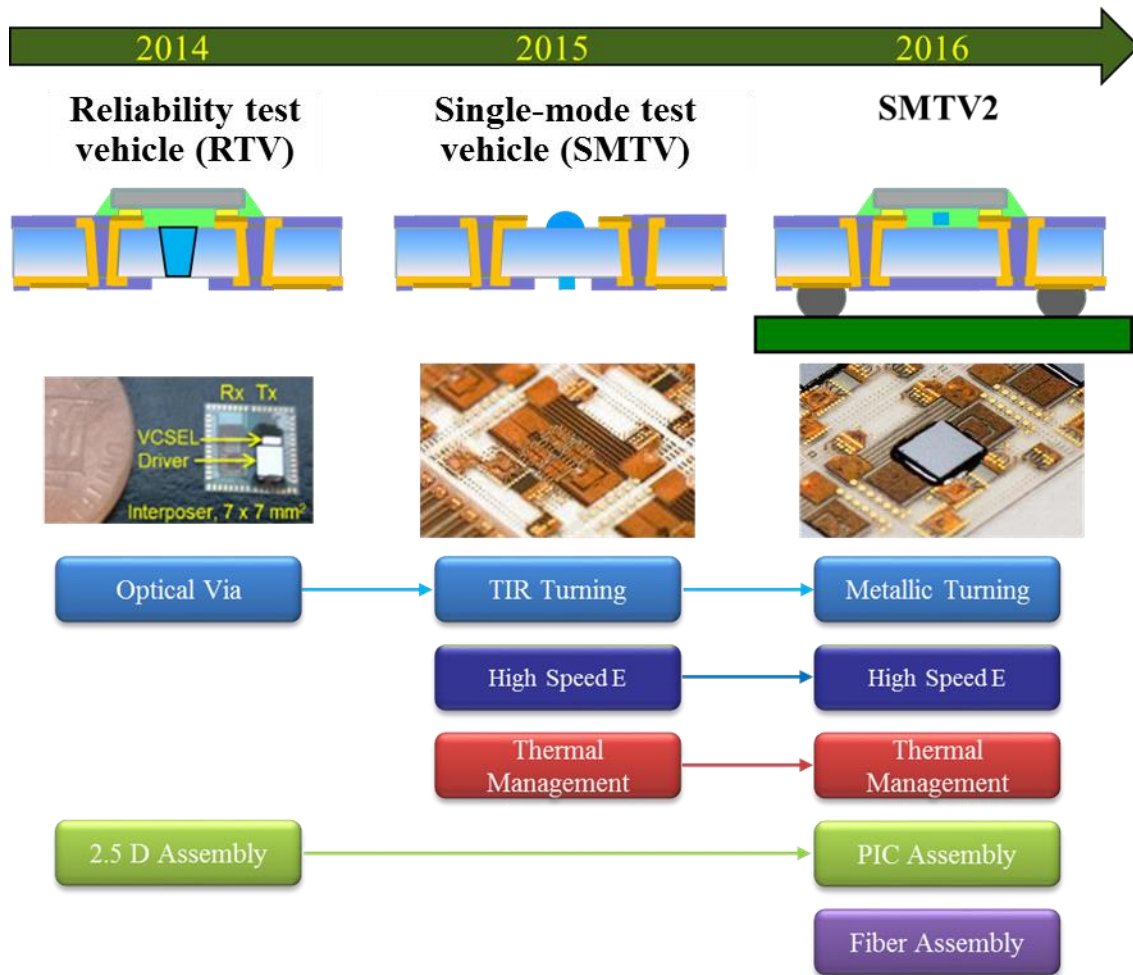
Two different out-of-plane turning structures have been studied: Total-internal-reflection (TIR) turning and metallic turning. Metallic turning structure is superior both in terms of coupling efficiency, fabrication tolerance, alignment tolerance, and long term reliability. While both turning structures have been fabricated, only metallic turning structure passes the fabrication tolerance and is testable. Optical measurement of the turning structure shows turning loss less than 2 dB, meeting one of the research objectives.

Two different fiber alignment groove structures have been studied: two-point contact u-groove and shallow cut u-groove. Neither groove structures were considered ready based on the results – both  $\Delta_y$  nor  $\Delta_z$  exceeded the 1-dB misalignment tolerance. Further research efforts are needed beyond the scope of this thesis.

## CHAPTER 5

### DESIGN AND DEMONSTRATION OF GLASS PHOTONICS MODULES

In this chapter, the optical interconnections presented in Chapter 3 & 4 are integrated in design and demonstration test vehicles (DDTV). The objective of the test vehicles is to emulate a photonics module based on its published design specifications and integrate building blocks in different disciplines in a glass photonics module. The roadmap of the test vehicles designed and demonstrated by the author is shown in Figure 5.1.



**Figure 5.1. Progression of test vehicles designed and fabricated for this thesis, and the building blocks implemented in each test vehicle**



At the writing of this thesis, all building blocks except for fiber assembly have been addressed. Although initial attempts in fiber assembly have been implemented in Single-mode Test Vehicle 2 (SMTV2), the results did not meet the passive alignment requirement. Addressing the single-mode fiber assembly challenge is beyond the scope of this thesis.

## **5.1 Reliability Test Vehicle (RTV) – Collaboration with TE Connectivity**

The first test vehicle is a collaboration with TE Connectivity, who provides VCSELs and drivers to fully assess the reliability of the solder joints and the performance of optical vias. Since the devices are designed for multimode optics, only the reliability results are relevant.

### **5.1.1 Design of RTV**

The design of RTV utilizes the VCSEL and the driver die per TE design. The VCSEL dies feature an array of 4 VCSEL diodes at 125  $\mu\text{m}$  pitch, designed for flip-chip bonding using 80:20 gold-tin (80Au20Sn) eutectic solder. The driver dies also feature an array for 4 channels designed to drive the VCSEL anode, but at 100  $\mu\text{m}$  pitch. The inputs to the driver are high speed differential signals designed for 10 Gbps operation, while the outputs from the driver to the VCSEL are single ended coplanar waveguides for the same bitrate. The driver is also designed for flip-chip bonding, but using tin silver (SnAg) solder instead. The area of the interposer is specified by TE, at 7 x 7  $\text{mm}^2$ . The edge of the interposer is lined by 300 x 500  $\mu\text{m}^2$  row of BGA pads. The high speed traces are from BGA to driver and from driver to VCSEL.

The reliability test studies 1) the Au-Sn joints between VCSEL dies and the copper pads, and 2) the tin silver joints between driver dies and copper pads, on glass interposer. The thermal cycling & thermal shock criterion is based on TE's requirement:

**1) Temperature Cycling Test (TCT): 100 cycles of -40 to + 85 C**

30 minute dwell time, cold temperature extreme first, 100 cycles. Temperature ramp rate > 10°C per minute (12.5 minute maximum transfer time). Allow specimens to remain at ambient conditions for at least 1 hour prior to obtaining performance data before and after the test.

**2) Thermal Shock Test: 15 cycles of 0 C to 100 C**

30 minutes dwell time, hot temperature extreme first, 15 cycles, 10 seconds maximum transfer time.

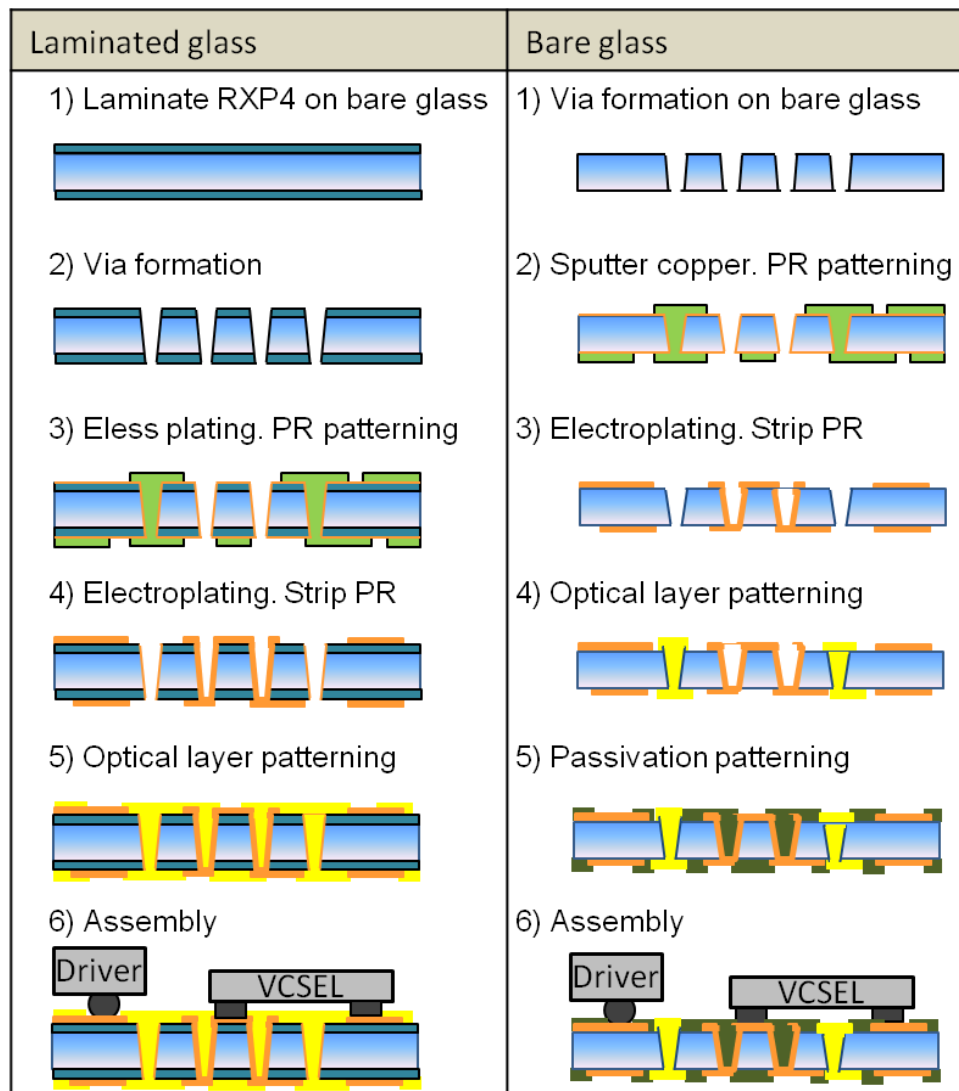
The thermal testing was performed in TE's facility after fabrication of interposer and assembly of dies at GT. The method to determine whether the joints pass the reliability testing are either through electrical testing, which is only possible for VCSEL dies, or through visual inspection. The methods for visual inspection are 3D microscopy or cross-sectioning. After cross-sectioning, the 2D plane can be observed through optical microscope, or through SEM. EDX can be performed (usually during SEM) to determine the material composition of the solder joints.

### **5.1.2 Fabrication of RTV**

The fabrication of glass interposer with through glass vias has been pioneered by GT PRC [72]. The process developed at PRC utilizes double side substrate fabrication process that are panel scalable, thus enabling low-cost fabrication. However, the standard process flow originally developed requires a polymer dielectric liner between glass and copper wiring. In order to take advantage of the low loss tangent of glass, an alternative process using direct copper metallization

on glass is preferred. As a result, bare glass metallization process was developed using sputter titanium-copper layer [73].

For the reliability study, both processes are investigated, as shown in Figure 5.2. Each step is described in detail in the following pages. The process steps are the same in later test vehicles so they will not be repeated unless otherwise noted.



**Figure 5.2. Process flow used for the reliability test vehicle**

## **Lamination of Dielectric Layer**

The dielectric layer used is an experimental material from Rogers Corporation, called RXP-4, which is similar to the RO4000 series materials available commercially [74]. The lamination process is by hot press, using a specific stack-up and process condition to ensure the glass panel does not crack during the pressing and the cooling process. The stack-up used included rubber layers on both sides of the glass. The process conditions are as follows:

- 1) Put stack up in hot press, engage, the ramp up to 250 C.
- 2) Increase pressure to 2 tons once the temperature exceeded 150 C.
- 3) Press for 90 min.
- 4) Decrease pressure to < 1 ton to let cool. When temperature is below 100 C, release pressure.

Any force cooling might potentially crack the glass.

## **Via Formation**

Through glass via (TGV) in this test vehicle was formed by Asahi Glass Company using ArF excimer laser ablation [75]. The short pulse width and high absorption of glass at the excimer wavelength enables one to form fine and precise TGVs with less thermal stress in glass. In addition, the formation of multiple TPVs over a large sample area is possible by mask projection technique. Via diameter of 30  $\mu\text{m}$  at 60  $\mu\text{m}$  pitch in a 100  $\mu\text{m}$  thick glass has been demonstrated using this technique.

## **Seed Layer Metallization**

For the laminated glass process, the seed layer was plated using Atotech's electroless plating chemistry. However, the desmearing steps used by Atotech for electroless plating has no effect on

RXP-4 so the associated process steps were replaced by an O<sub>2</sub> plasma etch to clean the surface of residue and increasing the surface energy.

For the bare glass process, Ti-Cu was sputtered on. The typical thickness is 100 nm Titanium adhesion layer and 300 – 500 nm copper layer.

### **Semi-Additive Process (SAP)**

SAP is consisted of eight steps:

1) Lamination of Hitachi dry-film photoresist using a roller laminator at 110 C at a relatively slow speed. The photoresist used in all fabrication steps in this thesis is 15 µm thick.

2) The mask for electrical wiring should be aligned to the vias. Once the mask is aligned, exposure at the correct dose is performed. For the 15 µm photoresist, the dose is 100 mJ/cm<sup>2</sup>.

3) 15 minute post exposure delay (PED). This will promote cross-linking of exposed photoresist.

4) Development in a NaOH solution. In PRC, the development of dry film photoresist is performed on a Chemcut semi-automatic developer.

5) The exposed copper surface needs to be cleaned of residue prior to electroplating. To do so, a cleaning stage is performed, first by dipping the sample into an alkaline cleaner solution, followed by water rinse, then acid dip to remove oxidation. The electroplating setup uses AC power, and the plating rate is a function of applied current and total area of the panel. To plate for 5 µm on a 100 x 100 mm<sup>2</sup> panel with 40 % copper coverage, 6 Amps of current for 20 minutes is typically required.

6) Once the desired thickness has been plated, the photoresist is stripped by an alkaline stripper solution to expose the seed layer.

7) Seed layer (as well as a thin plated layer) is removed using a Chemcut differential etcher.

8) Annealing of copper in convection oven, for 30 minutes at 180 C.

### **Optical Layer Patterning**

The optical layer was applied after SAP using CYCLOTENE™ 4026 liquid material, following the via filling and patterning process described in Chapter 3.

### **Passivation**

Dry film BCB material can work easily both as optical cladding and passivation. However, during 2014 this material was not available. As a result, Hitachi dry-film FZ series solder resist was used as passivation at that time [76]. The optimized process is as follows:

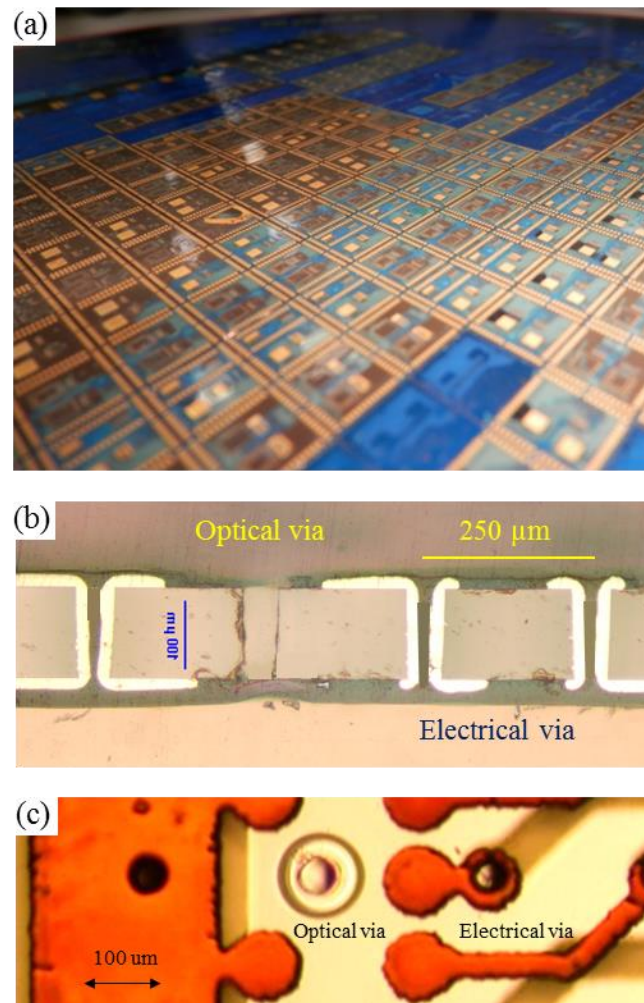
- 1) Vacuum laminator at 90 C, with 60 s vacuum time and 20 s pressure dwell time.
- 2) Align and expose at 180 mJ/cm<sup>2</sup>.
- 3) PED, 15 minutes.
- 4) Development in a NaOH solution. Once again, the development is performed on a Chemcut semi-automatic developer.
- 5) After development, surface residue should be removed using plasma cleaning with 4:1 ratio of O<sub>2</sub> and CF<sub>4</sub> for 5 minutes.
- 6) There are two curing stages. First is UV curing by flood exposure, of 1000 mJ/cm<sup>2</sup>. Second is thermal cure in a convection oven for 1 hour at 150 C.

### **Surface Finish**

Surface finish is needed to prevent the exposed copper surface from quickly oxidizing. For bonding to gold-tin eutectic, either ENIG (Electroless Nickel, Immersion Gold) or ENEPIG (Electroless Nickel, Electroless Palladium, and Immersion Gold) can be applied. In this test

vehicle, ENEPIG is used to prevent potential Nickel migration. The ENIG and ENIPIG processes are based on wet chemistry provided by Atotech.

The fabricated results are highlighted in Figure 5.3.



**Figure 5.3. Fabrication highlight of the 2.5 D reliability test vehicle. (a) Panel view showing 7 x 7 mm<sup>2</sup> interposers, (b) close up cross-section of optical and electrical vias in glass interposer, and (c) close up top view of the vias with VCSEL pads prior to application of passivation layer**

### 5.1.3 Assembly of Active Devices

The assembly of VCSEL and Driver dies is challenging due to the incompatible interconnection technology: AuSn eutectic point is at 280 C, as shown in the phase diagram in Figure 5.4, while the SnAg reflow temperature is around 250 C. To resolve the incompatibility, the VCSEL dies are assembled and reflowed first, followed by the assembly and reflow of Driver dies.

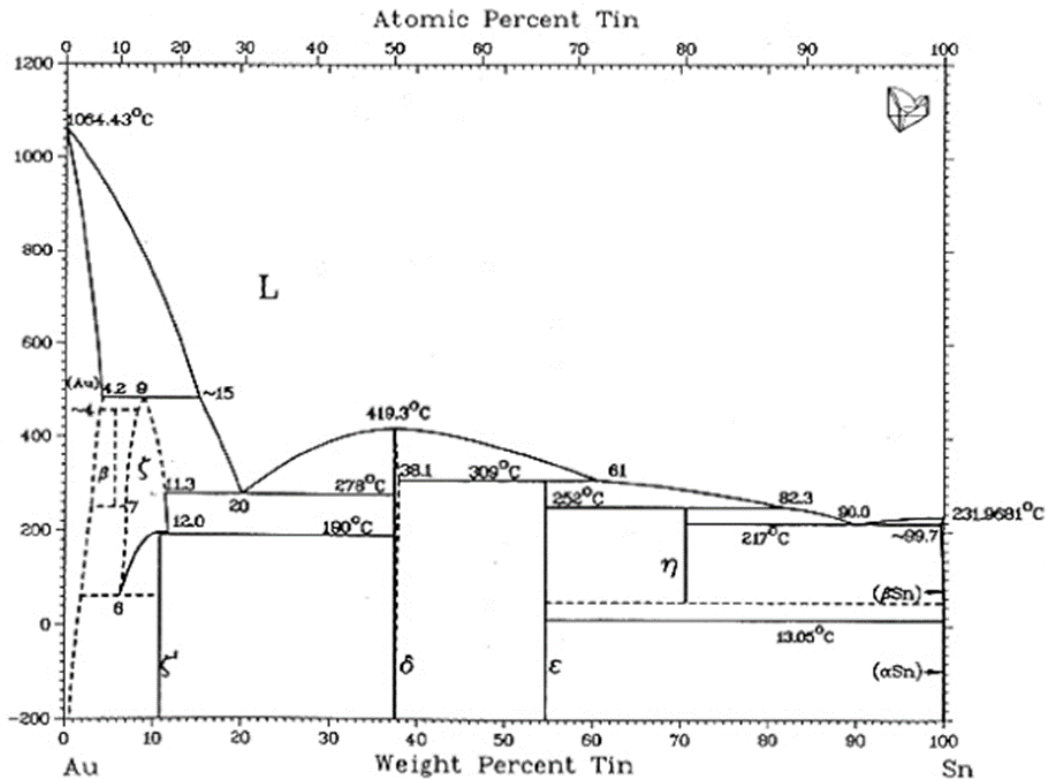


Figure 5.4. Phase diagram of Au – Sn compound [77]

### Au-Sn Diffusion Modeling

The Au-Sn solder is plated sequentially on top of a Nickel barrier layer at the surface of VCSEL dies. The thickness of Au layer is around 11  $\mu\text{m}$  and the thickness of Sn layer is around 4  $\mu\text{m}$ . Au-



Sn Intermetallic (IMC) is a diffusion limited process, and can be modeled by Fick's first law as a function of reflow temperature and time:

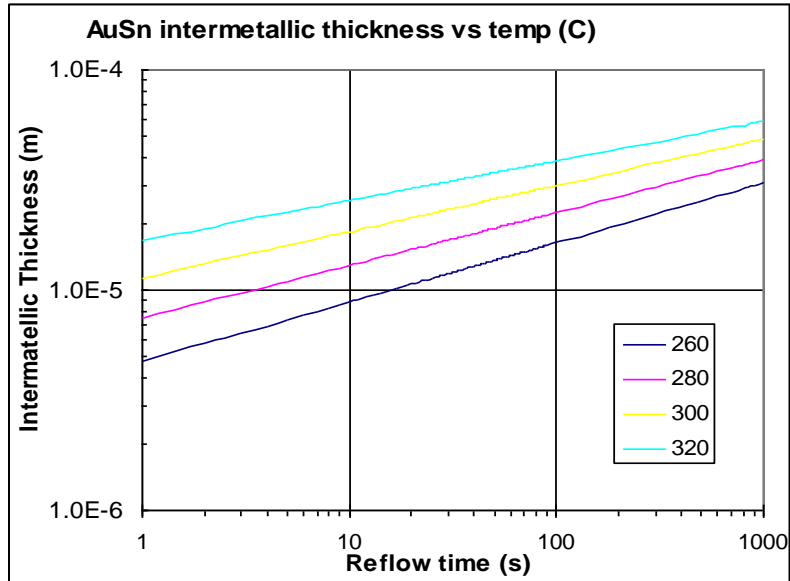
$$l = k \cdot \left( \frac{t}{t_0} \right)^n \quad \begin{array}{l} l = \text{total intermetallic thickness} \\ t_0 = \text{reference time} = 1 \\ n = \text{time exponent} = 0.25 \end{array} \quad (5.1)$$

Where  $k$  is the diffusion coefficient described by the Arrhenius relationship:

$$k = k_0 \cdot \exp\left(-\frac{Q}{RT}\right) \quad \begin{array}{l} k_0 = \text{intrinsic diffusivity} = 1.33 \\ Q = \text{activation energy} = 55.6 \text{ kJ/mol} \\ T = \text{temperature (Kelvin)} \\ R = \text{gas constant (8.3114 J/mol-K)} \end{array} \quad (5.2)$$

Based on the above numbers, the IMC thickness as a function of reflow time can be plotted against different temperatures as shown in Figure 5.5. As can be seen from the plot, the desired reflow time for 15  $\mu\text{m}$  of IMC is 20 s at 300 C, and 60 s at 280 C.

The time above is the theoretical minimum. In reality, there are several process related variations that may cause the eutectic temperature to shift: the chipping of as plated tin layer during transfer and handling, the planarity of the gold pad on glass interposer, and the warpage of glass interposer during assembly, which is studied next.



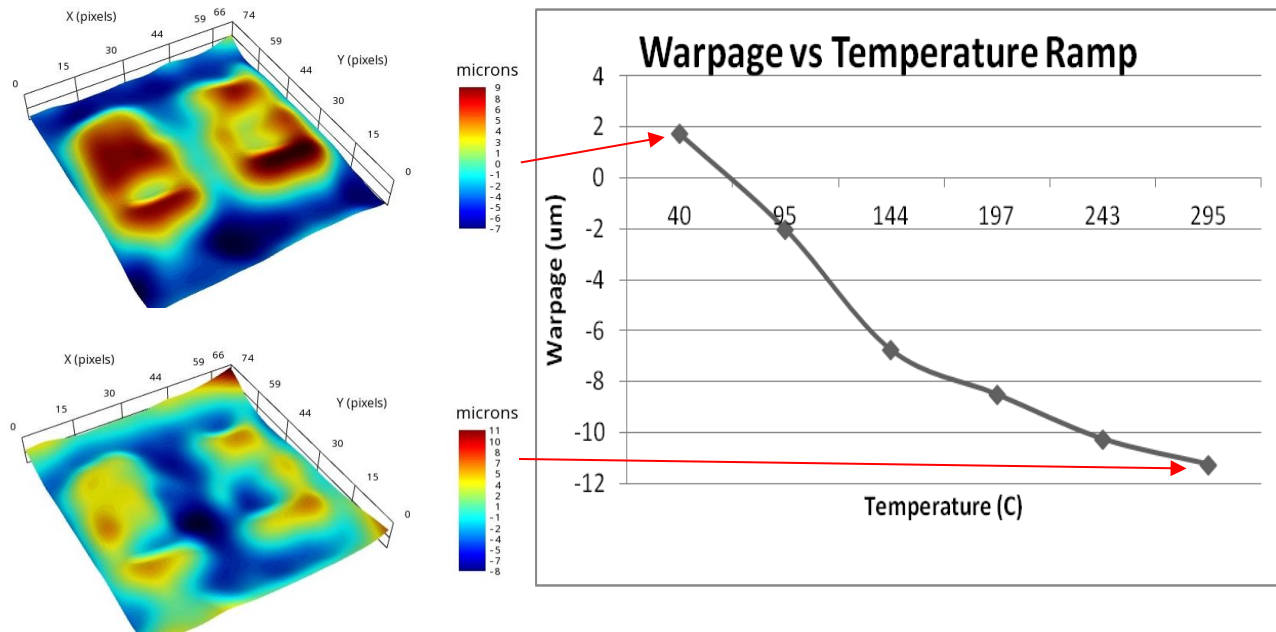
**Figure 5.5 Thickness vs. diffusion time of Au-Sn IMC formation**

### Glass Warpage Study

The warpage of the interposer plays a major role in landing all of the solder joints of the dies during assembly. The warpage of a  $7 \times 7 \text{ mm}^2$  glass interposer fabricated using bare glass stack up is measured at different temperatures, to assess the risk during reflow assembly. The warpage vs temperature ramp is plotted in Figure 5.6. In here, the warpage is defined as:

$$\text{Warpage} = \text{center height} - \text{average height of the four corners.}$$

The warpage is only  $2 \mu\text{m}$  at room temperature. During ramp to  $300 \text{ C}$ , the warpage increases to  $12 \mu\text{m}$  across the  $7 \times 7 \text{ mm}^2$  interposer. However, this is the warpage from the center of the interposer to the corner, for a VCSEL die, the warpage from one end of the die to the other is less than  $1/3$  of that amount. In another word, the substrate warpage from one end of the VCSEL die to the other is about  $4 \mu\text{m}$ . While this is not insignificant for a  $20 \mu\text{m}$  bump, during reflow all of the bumps should land normally. Therefore, warpage is considered tolerable for the bare glass stack up. The warpage of the laminated glass stack up was not measured since the bare glass stack up was determined to be the process of record.



**Figure 5.6. Warpage measurement of bare glass interposer at different temperatures**

### Planarity of Gold Pad

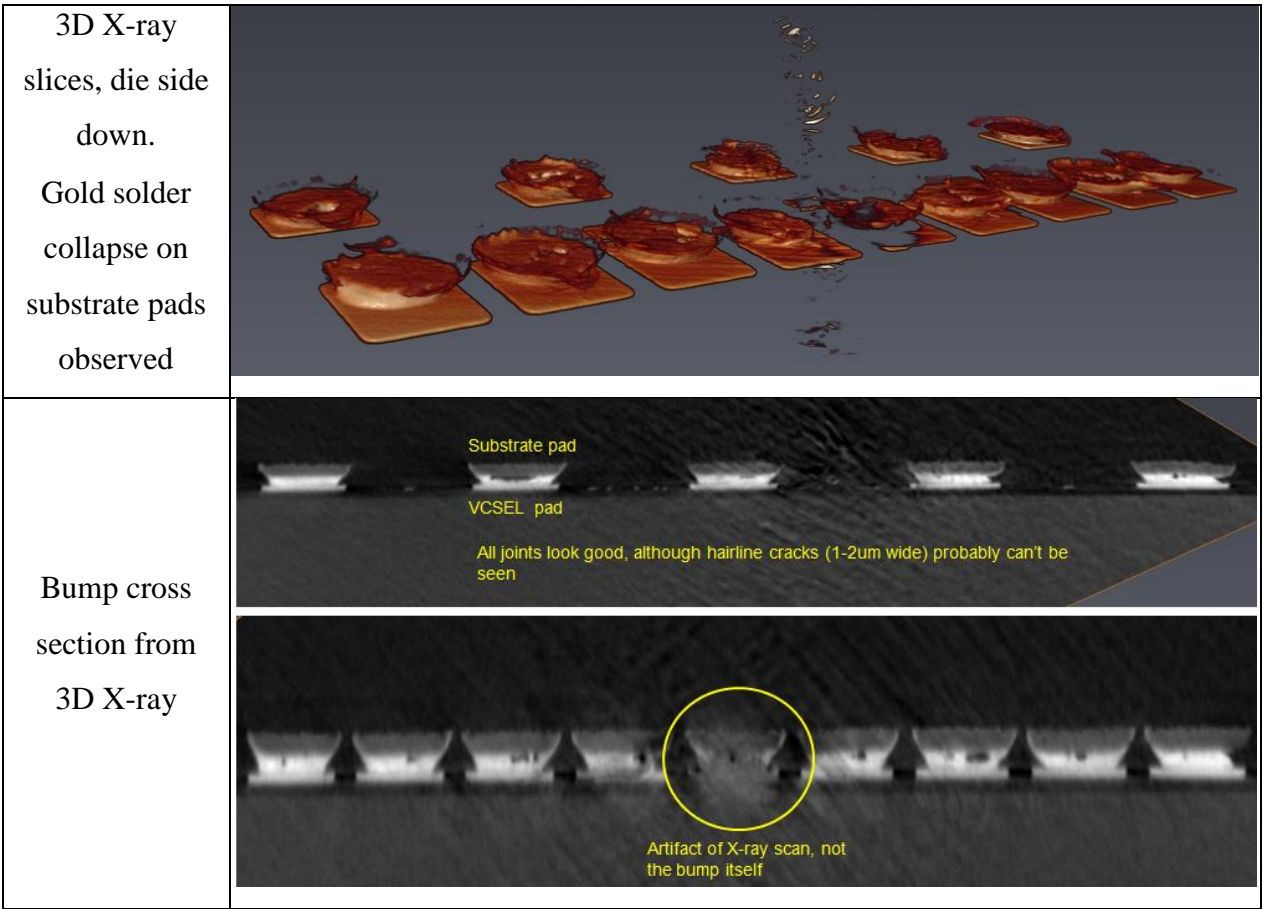
If the gold pad is not planar within the bonding region, the Au-Sn solder will collapse and form undesirable IMC. To validate this, 3D X-ray microscopy is performed on one of the assembled VCSEL dies, and the results are shown in Figure 5.7. Unfortunately, the gold pads on glass substrate is not planar and visible collapse is observed on all pads. To address this issue, the pads must be passivation following Solder Mask Defined (SMD) design rules.

After switching to SMD pad opening, gold solder collapse is under control. However, the chipping of plated Sn during shipping and handling is still a concern with no easy solution in a research lab setting.

The assembly of driver, in comparison, is low risk as glass warpage within the driver die area is only 5 μm during reflow optimized process flow, and the SnAg solder is already reflowed so it

is not as sensitive to surface damage during transfer. The optimized assembly process is documented in Table 5.1.

The assembled samples are highlighted in Figure 5.8.

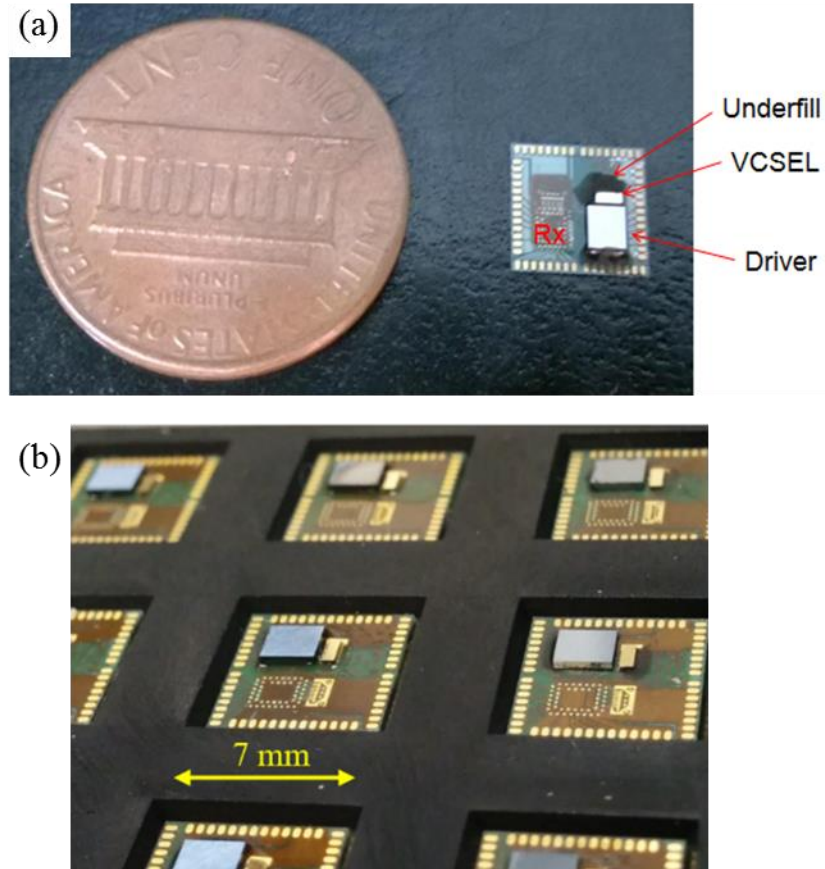


**Figure 5.7.** 3D X-ray scan of Au-Sn joint after VCSEL assembly to gold pads on glass interposer

**Table 5.1.** Optimized 2.5 D assembly process condition

Step	Conditions
Clean & dry	Acetone rinse. Then bake at 150 C for 30 mins.
VCSEL assembly	Reflow at 300 C, 45 s, with forming gas & flux, on SMD pads.
Driver assembly	Reflow at 250 C, with flux, on SMD pads.

Clean & dry	Acetone rinse to remove flux. Then baked at 150 C for 30 mins.
Underfill	Dispensing underfill at room temperature and fill by capillary action.
Thermal cure	150 C, 1 hour, in convection oven



**Figure 5.8. Assembled 2.5 D optical reliability test vehicle (a) compared against a penny and (b) arranged in a box for reliability study**

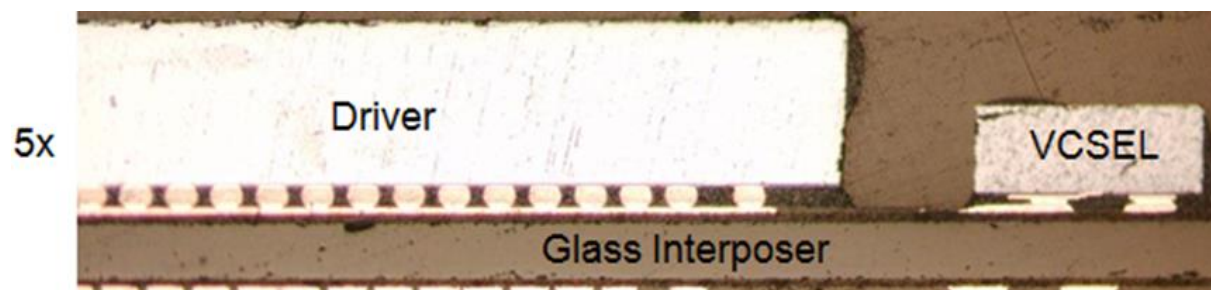
#### **5.1.4 Reliability Study of Actives Devices**

Reliability testing according to TE's specification, described in 5.1.1, was performed on 10 assembled samples.

The solder joint reliability is assessed by electrical measurement of the VCSEL pads – a change in VCSEL resistance during forward biasing indicates potential solder joint failure. Of all of the VCSELs that were measured at time zero, all passed 100 TCT without any failure.

To dive deeper, optical observation using SEM and EDX is the best option. One interposer each after 100 TCT and Thermal Shock, is cross-sectioned and observed under optical microscope.

The sample after 100 TCT is shown in Figure 5.9. The SnAg solder on the driver side shows necking on the interposer side, but there's no significant voiding. The VCSEL shows observable hairline cracks. There are some amounts of remaining Au and non-wet areas, which may be caused by bumps non-coplanarities, excessive fluxing, or pad surface roughness.



**Figure 5.9. Cross-section of VCSEL and Driver dies after 100 TCT**

The sample after thermal shock is shown in Figure 5.10. The SnAg solder on the driver side shows necking on the interposer side similar to 100 TCT case. The VCSEL again shows adequate integrity although with small but non-fatal hairline cracks. The usual remaining Au and voids can all be attributed to the same source of bumps non-coplanarities.

For all three cases, the observable failure mechanisms are the same and are present at time zero already. In other words, they are not caused by reliability testing, but rather were inherent to the process or the dies. In the case of VCSEL dies, the voids are likely caused by the surface quality

of plated Au-Sn layer. On the other hand, the high Au concentration is likely due to the reflow profile not being optimized. The hairline cracks, necking, and non-wetting are likely due to warpage and surface quality of the interposers.



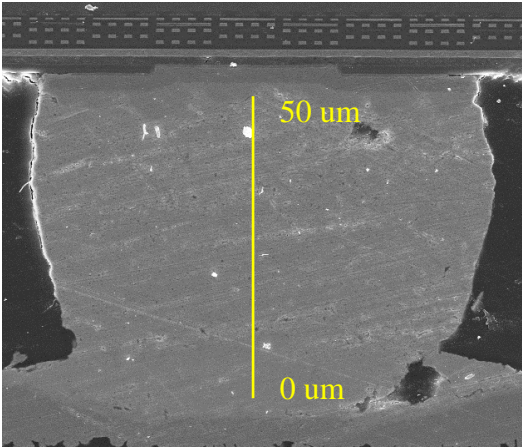
**Figure 5.10. Cross-section of VCSEL and Driver dies after thermal shock test**

SEM and EDX scan of the driver joints before and after reliability testing is shown in Figure 5.11. The distribution of silver is along the top and bottom interfaces, and no trace of IMC from Cu, Pd, or Ni was observed. The SEM and EDX scan of the VCSEL joints before and after reliability testing is shown in Figure 5.12. The distribution of Au<sub>5</sub>Sn (light color) and AuSn (dark color) phases can be clearly observed from the SEM picture. The composition seems to be slightly off eutectic for both cases, which can be attributed to the same substrate or die non-idealities described before. No undesirable IMC (with Cu or Ni) was detected.

In summary, the reliability testing was successful. This concluded the main objective of the reliability test vehicle.

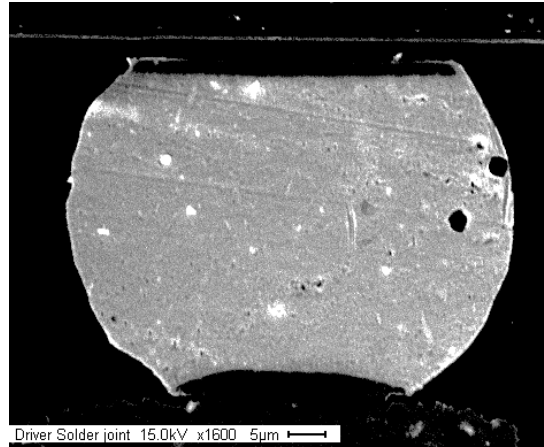


Time zero



Height (um)	Sn	Ag
50	100	0
33	100	0
17	100	0
0	94	6

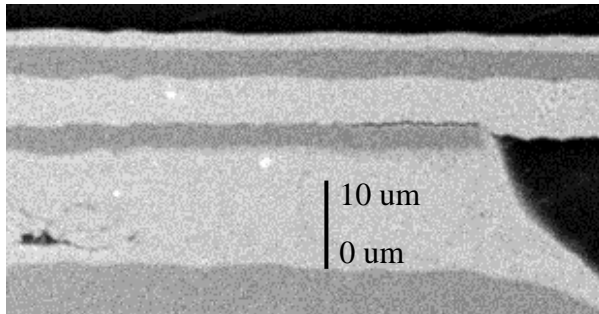
After thermal shock



Height (um)	Sn	Ag
50	94.3	5.7
33	100	0
17	100	0
0	98.5	1.5

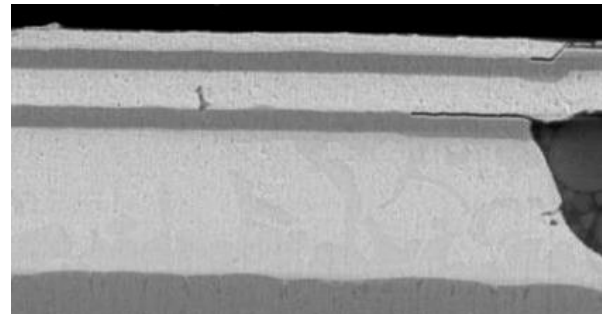
**Figure 5.11. SEM & EDX of driver solder joint between time zero and post thermal shock**

Time zero



Height	Au	Sn	Ni
10	81.4	18.6	0
6.67	87.47	12.53	0
3.33	71.32	28.68	0
0	89.18	10.82	0

Post 100 TCT



Height	Au	Sn	Ni
10	69	31	0
6.67	89.76	10.24	0
3.33	88.3	11.7	0
0	48.33	38.54	13.14

**Figure 5.12, SEM & EDX of VCSEL solder joint between time zero and post 100 TCT**

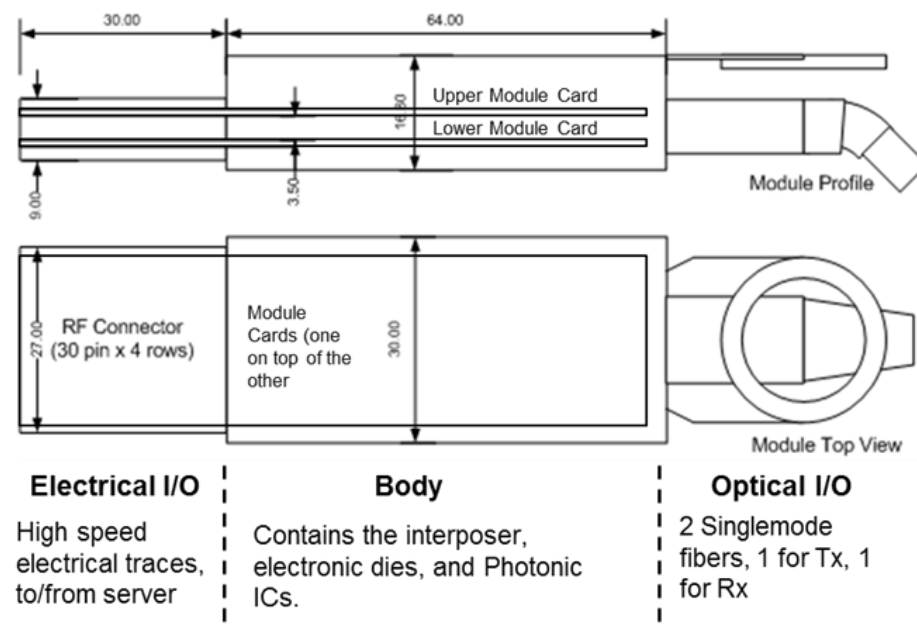


## 5.2 Single-Mode Test Vehicle (SMTV & SMTV2)

The single-mode test vehicle (SMTV) is a collaboration between GT PRC, Ciena Corporation, and TE Connectivity. The goal of the collaboration is to demonstrate an optical transceiver module using glass interposer technology based on CDFP multi-source agreement (MSA). The scope of the demonstration involves design and characterization of optical, electrical, and thermal interconnects. There are two generations of the single-mode test vehicle (SMTV & SMTV2) – one was delivered in fall 2015, while the second one is to be completed in fall 2016.

### 5.2.1 Design of SMTV

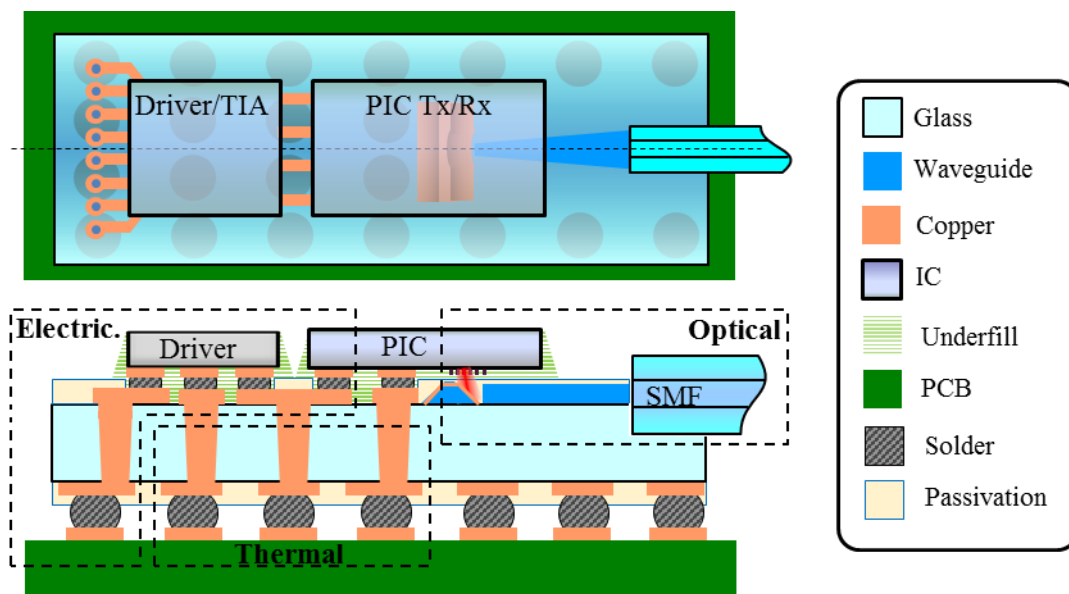
Unlike the reliability test vehicle where the design was provided by TE, the design for SMTV is started from scratch from the CDFP MSA. The MSA specified the body of the pluggable as shown in Figure 5.13.



**Figure 5.13. CDFP Type II body, with two module cards shown**

The intention of the MSA is to split the transmit (Tx) and the receive (Rx) into two module cards, such that the Upper Module Card contains Tx and the Lower Module Card contains Rx. The RF Connector on the left end is the **Electrical I/O** interface to and from the server, it contains 64 high speed electrical traces – 16 differential pairs each for the Tx side and for the Rx side. Each differential pair is expected to operate at 25 Gbps. The length of the electrical I/O portion (30 mm in this drawing) provide room for thermal dissipation and pluggable form-factor.

The MSA indicated that single-mode implementation utilizing dense wavelength division multiplexing (DWDM) is preferred, so that the 16 electrical channels are combined in the optical domain into a single fiber for each of Tx and Rx. A 2.5 D glass interposer approach utilizing a silicon chip adjacent to a silicon photonic integrated circuit (PIC) chip is proposed as shown in Figure 5.14.



**Figure 5.14. Proposed 2.5 D module card design using glass interposer, with optical, electrical, and thermal interfaces**

The chip specifications are provided by Ciena Corporation in a Bill of Materials (BOM). The silicon chip is the electrical driver at the Tx end, and the trans-impedance amplifier (TIA) at the Rx end. The PIC consists of optical circuitry to implement DWDM such as array waveguide gratings (AWG) and vertical grating couplers (VGC). In addition, edge emitting lasers (EEL) are bonded on the Tx side. There are other components, such as the micro-controller and the voltage regulator module, in the BOM; however, they are not speed sensitive and can reside on the PCB. The Bill of Materials with only these four devices is shown in Table 5.2.

**Table 5.2. Simplified Bill of Materials for dies on glass for SMTV**

Device Name	Qty.	# I/O	L x W (mm)	Optical	I/O Pitch	Description
Tx PIC	1	300	4 x 5.5	Si WG 1 VGC	125 $\mu$ m	Integrated Lasers (16x), EAM (16x), Optical Multiplexer (1x)
Rx PIC	1	100	6 x 6	Si WG 1 VGC	125 $\mu$ m	Photo-Detectors (16x), Dual-Pol De-multiplexer (2x)
Driver	4	60	2 x 1.6	N/A	150 $\mu$ m	EAM Mod Driver (4x)
TIA	4	50	1.5 x 3	N/A	150 $\mu$ m	TIA + CDR, clocking (4x)

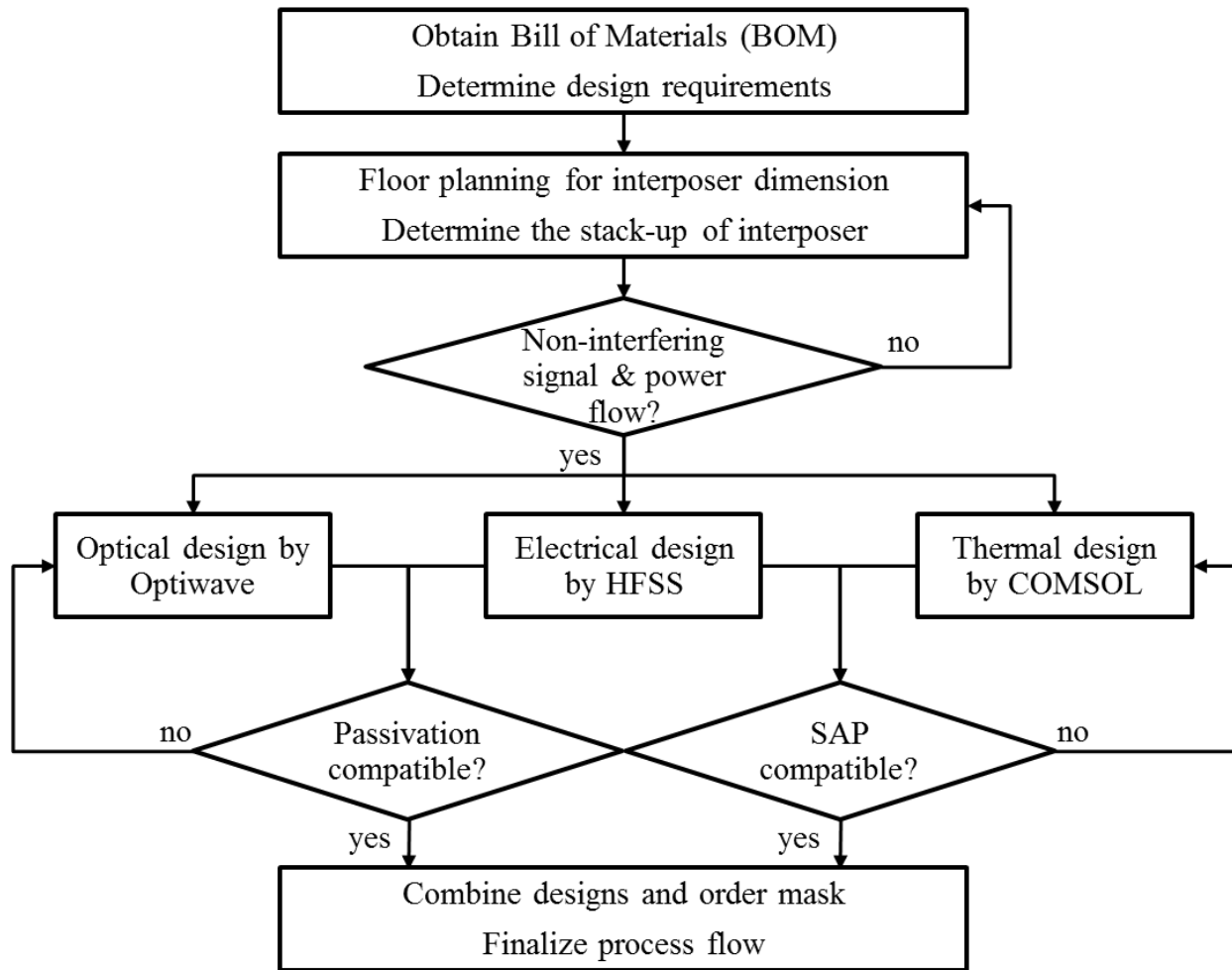
The design requirements for the optical, electrical, and thermal interconnects for SMTV is shown in Table 5.3. Optically, only one vertical grating coupler is used for each of the Tx and Rx PIC. There's no optical loss budget, so a target of < 3 dB is used based on literature [78]. The metallic turning structure presented in Chapter 4 is willed to meet the loss budget. Electrically, the

pitch of the high speed differential traces is to match the pitch of Driver and TIA, and the differential impedance of the traces needs to be  $100\ \Omega$ . In addition, the propagation loss ( $S_{21}$ ) and return loss ( $S_{11}$ ) of these traces should be within conventional signal integrity targets of  $< 1\ \text{dB/mm}$  and  $> 20\ \text{dB}$  at 28 Gbps. Also of interest is the minimum trace spacing where the crosstalk is  $< 30\ \text{dB}$ . Thermally, all active devices must be kept cool during operation. In particular, the EELs on the PIC-Tx is most sensitive, and must be kept under  $80^\circ\ \text{C}$  during normal operation.

**Table 5.3. Interconnect design requirements in SMTV**

Interconnect	Design Requirement		Approach
Optical	Loss	3 dB	Metallic turning structure as shown in Chapter 4
	Turning angle	$45^\circ$	
Electrical (high speed losses are rated at 28 Gbps)	Pitch	150 $\mu\text{m}$	Electroplated microstrip lines (MSL) directly on glass
	Differential impedance	$100\ \Omega$	
	Return loss	$> 20\ \text{dB}$	
	Propagation loss	$< 1\ \text{dB/mm}$	
	Crosstalk	$< 30\ \text{dB}$	
Thermal	PIC temperature	$< 80\ \text{C}$	Thermal via arrays
	Driver temperature	$< 85\ \text{C}$	

Since there are three different types of physics, a co-design strategy is developed to meet the requirements for each. The flow chart for the co-design strategy is shown in Figure 5.15. The first step has been described in this section already. The rest will be covered next.



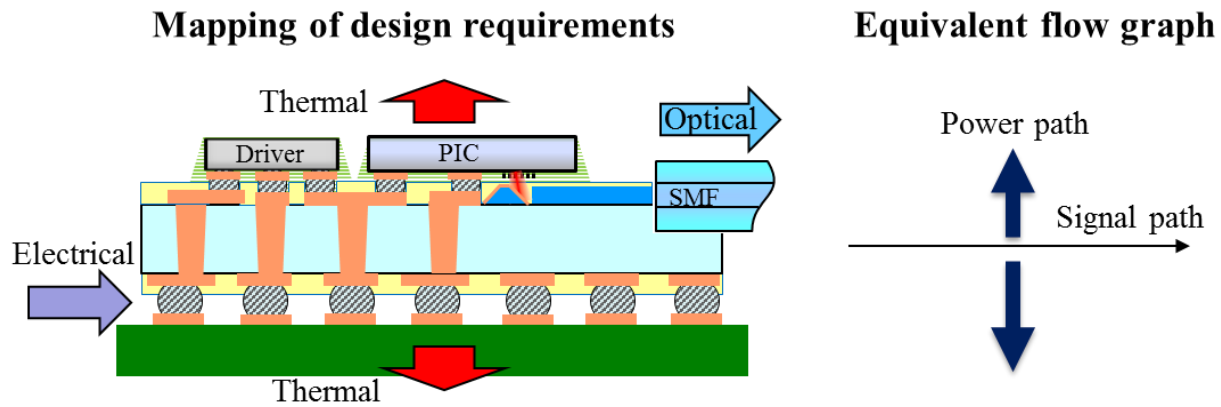
**Figure 5.15. Co-design flow chart for SMTV**

### 5.2.2 Floor Planning of SMTV

The dimension of the glass interposer is determined based on floor planning. The first step in floor planning is the 2D mapping of design requirements into an equivalent flow graph to clearly separate noisy power lines from sensitive signal lines, as shown in Figure 5.16.

The next step is in allocating all signal lines from top. Since the dies are larger in the Rx side, this exercise is done in the Rx side. Rx connection between the PIC and TIA need to be a matched transmission line with a minimized length. The 1 x 4 TIA is oriented such that the short end must

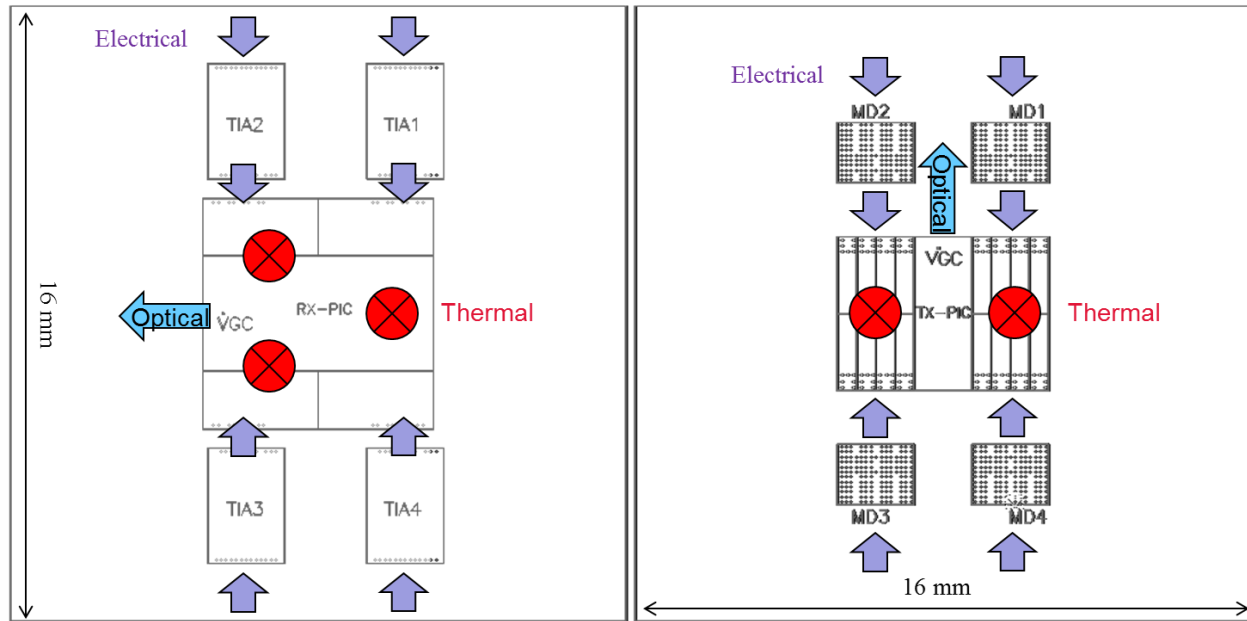
interface the PIC. Enough space is needed to allow routing of high speed differential signals from Which means the maximum width considering the long end of TIA is  $6\text{ mm} + 2*0.5\text{ mm}$  (PIC to TIA trace) +  $2*3\text{ mm}$  (long end of TIA) +  $2*1.5\text{ mm}$  (space reserved for routing) =  $16\text{ mm}$ . As a result, the size of the interposer is set at  $16\text{ mm} \times 16\text{ mm}$ .



**Figure 5.16. Equivalent flow graph for SMTV**

On the other side of the glass, the number of BGA balls need to be on par with the I/O counts as a rule of thumb. The number of I/O on the Tx side is  $300 + 60*4 = 540$  pins. At  $500\text{ }\mu\text{m}$  pitch, the number of BGA balls that can be achieved within a  $16\text{ mm} \times 16\text{ mm}$  interposer, with  $500\text{ }\mu\text{m}$  keep out, is 961, which is much larger than 540. Therefore, interposer size is not BGA limited.

Shown in Figure 5.17 is the floor planning results for both the Tx and Rx end, centered within a  $16\text{ mm} \times 16\text{ mm}$  glass interposer, showing direction of optical, electrical, and thermal interconnects.

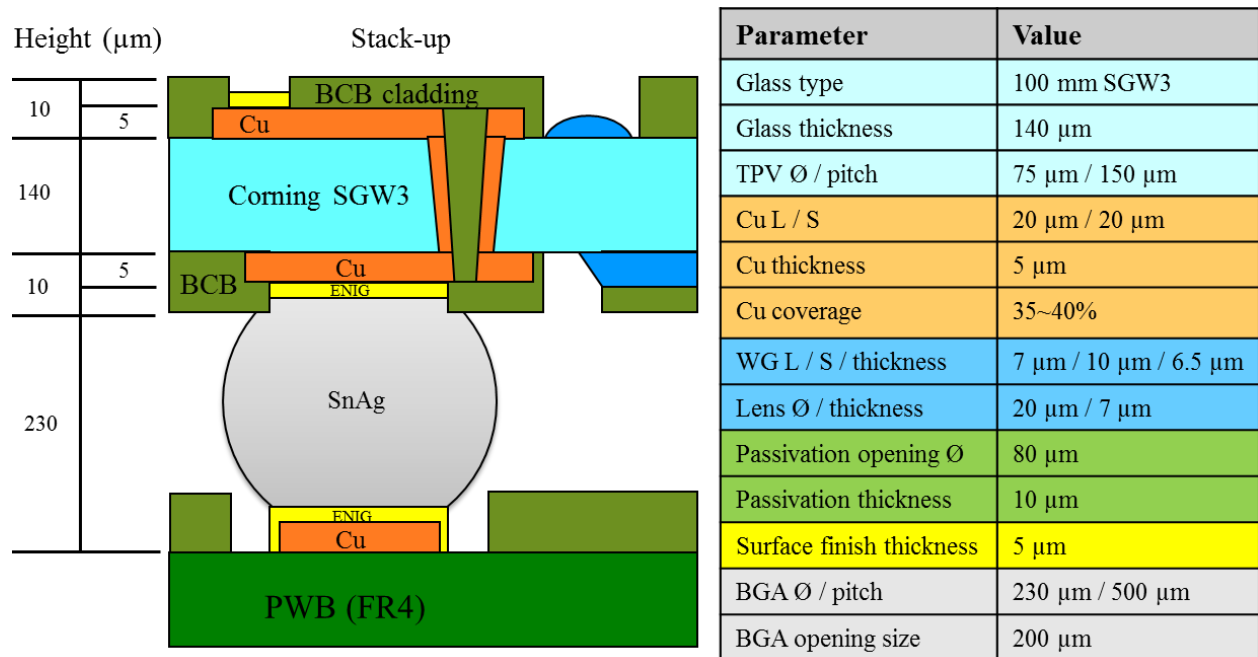


**Figure 5.17. Interposer floor planning based on BOM and signal/power flow graph**

### 5.2.3 Test Vehicle Stack-Up

The stack-up of the test vehicle is chosen based on the glass interposer technology available at Georgia Tech. The bare glass process developed for the reliability test vehicle described in Figure 5.2 is used as the basis. The BGA technology chosen is 500  $\mu\text{m}$  pitch, with a targeted ball diameter of 230  $\mu\text{m}$ . The proposed stack-up is shown in Figure 5.18. This figure is drawn for the first generation test vehicle (SMTV) where TIR turning with micro lens is used. For the second generation test vehicle (SMTV2) the stack-up is actually simpler because the optical layer only exist on the top side of glass. Lastly, unique fabrication process steps need to be developed to optimize optical, electrical, and thermal interconnects.

Once the floor planning and the stack-up are determined, the each interconnect is designed simultaneously.



**Figure 5.18. Stack-up of SMTV**

## 5.2.4 Modeling of SMTV

Three different types of modeling tool are used to address the optical, electrical, and thermal design requirements. Although COMSOL has the capability to model all physics involved using finite element method (FEM), the mesh size required for each physics is on a completely different scale. For optical simulation, the mesh size needs to be between 10 to 50 nm to capture precise grating periods of Vertical Grating Couplers (VGC). For electrical simulation, the mesh size is set by the finest electrical feature, which is usually the thickness of copper metallization (5  $\mu\text{m}$ ), to be between 0.5 to 2  $\mu\text{m}$ . For thermal simulation, the precise topology of electrical wiring does not have a strong effect on overall dissipation and can easily overburden the computing resources. Unit cells using equivalent thermal conductivities, which are more than 100  $\mu\text{m}$  in dimension, are used in place of precise topology to capture the heat dissipation. Since the mesh sizes are two order of magnitude different, there is no real advantage in modeling using the same software.



Optiwave has been used by the author for optical modeling, with the results already presented in Chapter 3 and Chapter 4. Ansys HFSS (High Frequency Structural Simulator) is chosen for electrical modeling because it has been widely used in PRC for analysis of high speed transmission lines in glass. COMSOL with equivalent model is chosen for thermal modeling because of its ease of implementation.

### **Optical Modeling**

The optical modeling and design of the test vehicle include both the TIR turning structure and the metallic turning structure, which have already been presented in Chapter 4.

### **Electrical Modeling**

The goal of the electrical design is to develop high yield design rules that meet both the design requirements as well as the process requirements. A flow chart is used to help develop high yield electrical design rules, as shown in Figure 5.19. To start, a wide range of microstrip line (MSL) pairs are parametrically swept across different dimensions to determine the differential impedance. For an MSL differential pair, the dimensions of interest are W, the width of the traces, S, the spacing between the pair, h, the thickness of the dielectric layer, and t, the thickness of the traces. In this test vehicle, h & t are set. Therefore, the only variables are W & S. The parametric study for W & S is shown in Figure 5.20. As shown, many combinations of W & S can make 100 ohm differential.

The next step is to match the pitch with the chip bump pitch, which is 150  $\mu\text{m}$ . Clearly, the combination of W = 100  $\mu\text{m}$  and S = 50  $\mu\text{m}$ , with the single-ended impedance = 70  $\Omega$ , is the best choice. 3D EM simulation follows to determine the propagation and return losses.

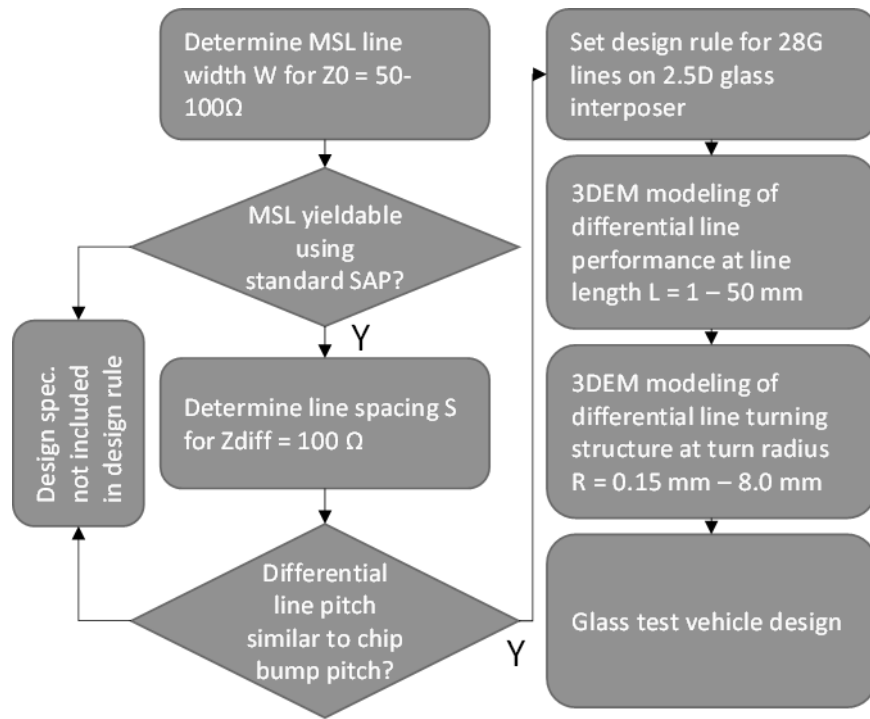


Figure 5.19. Modeling approach to develop high yield electrical design rules [79]

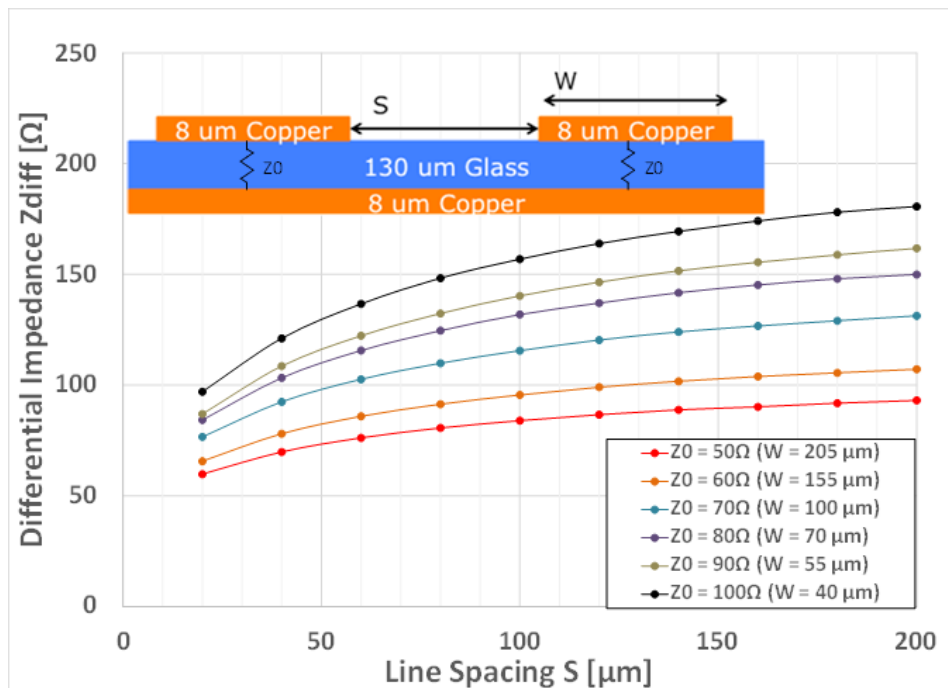
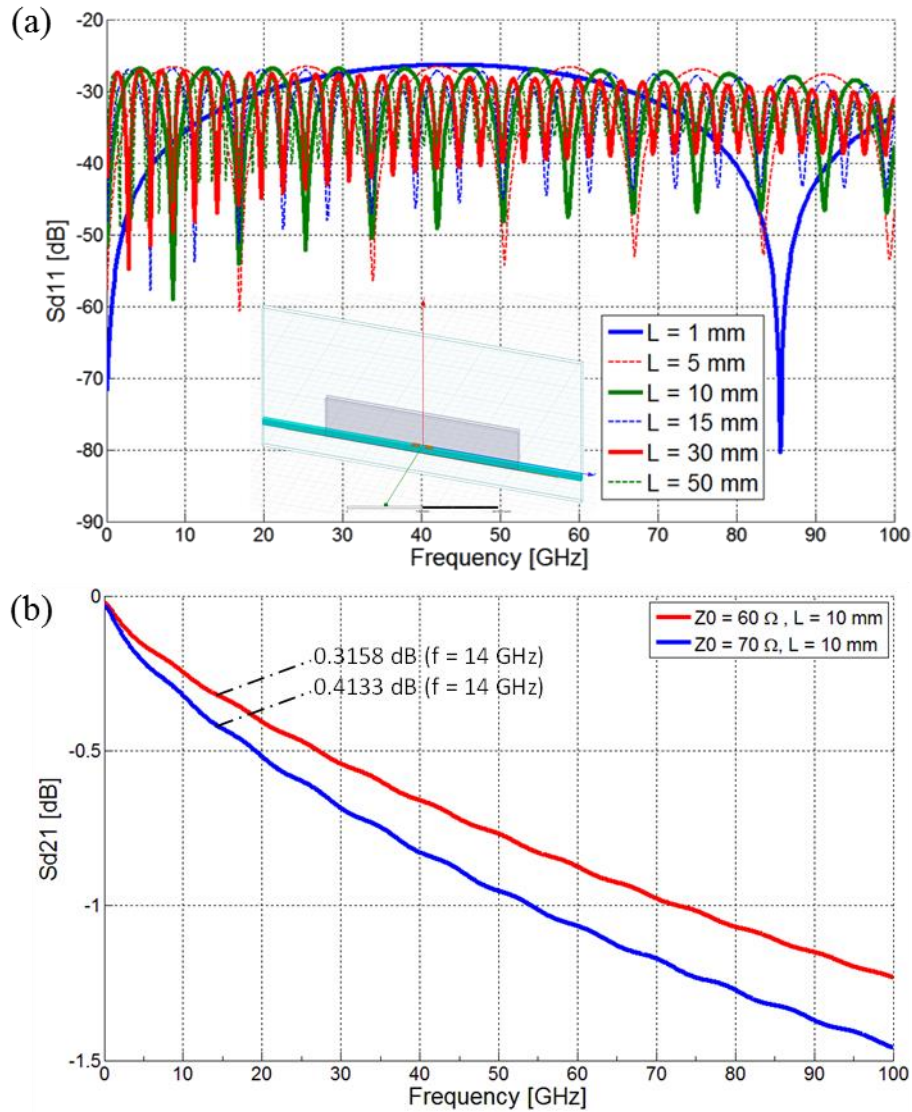


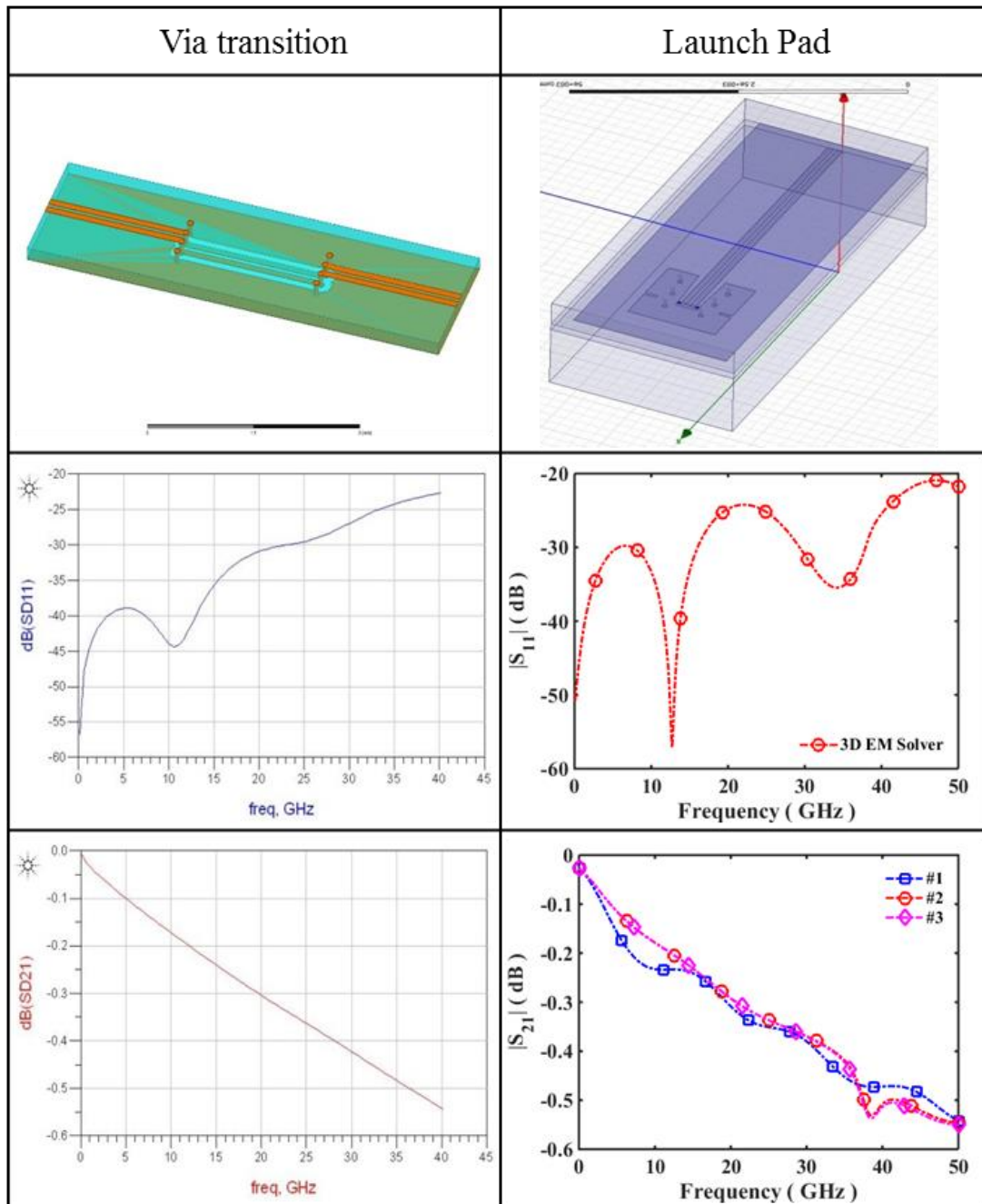
Figure 5.20. 2D EM extraction of interposer stack-up to determine differential line impedance (glass thickness and copper thickness are slightly different)

The 3D EM simulation results are shown in Figure 5.21. The return loss of MSL lines are all under 25 dB all the way up to 100 GHz, including the Nyquist frequency of  $28/2 = 14$  GHz. On the other hand, the propagation loss is less than 0.05 dB/mm, which is an order of magnitude lower than the target. 3D EM modeling is also performed on via transition structures and termination structures, as summarized in Table 5.4.



**Figure 5.21. 3D EM modeling of (a) the return loss and (b) propagation loss of the MSL used in SMTV**

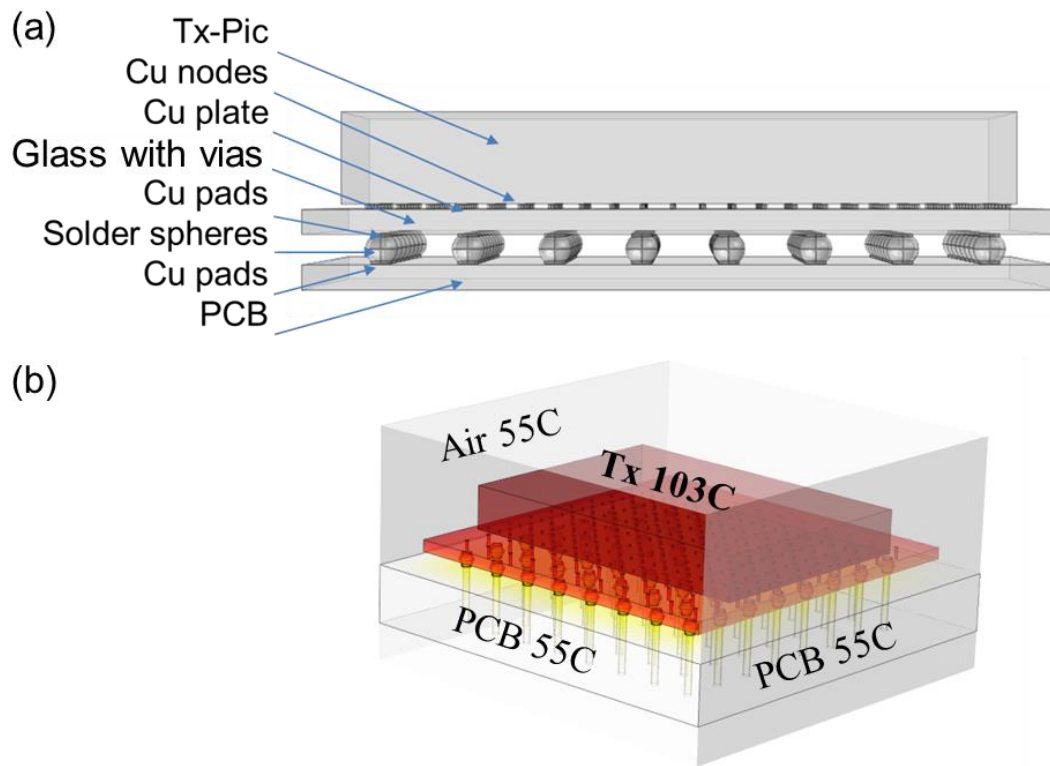
**Table 5.4. 3D EM modeling of via transition and high speed launch pad structures. The  $S_{11}$  is well under -25 dB at 14 GHz, and the  $S_{21}$  is well under 1 dB at 14 GHz. Design of high speed launch pad is courtesy of Ciena Corporation**



## Thermal Modeling

The goal of the thermal design is to dissipate enough heat from the dies to maintain their operating temperature to a recommended value. While the recommended temperature is under 90° for all active devices, PIC-Tx has the most stringent requirement: the lasers must be kept at below 80° during operation, when the PIC-Tx die is expected to output 6.7 W of power. The ambient temperature is assumed to be 55°.

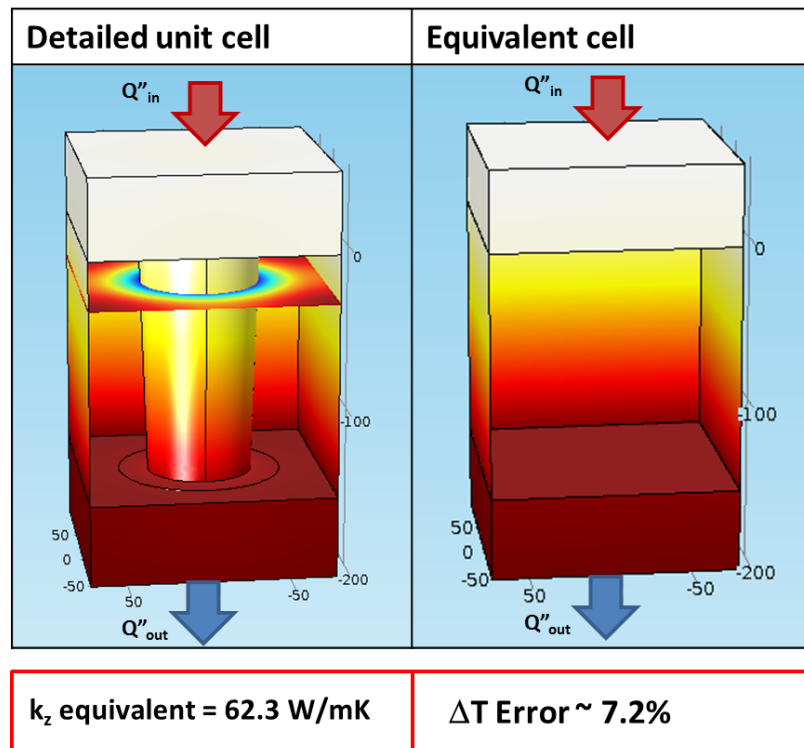
Initial 3D modeling of PIC-Tx heat dissipation is shown in Figure 5.22. The emitted power on die is not dissipated very well through glass, resulting in > 100 C operating temperature.



**Figure 5.22. 3D COMSOL modeling of PIC-Tx only, at 500  $\mu\text{m}$  thermal via pitch**

There are a few concerns with the model above. First, only a small space is modeled due to concerns for computation space. In fact, the dimension of the model is 5 mm x 5 mm x 3 mm. Recall from Figure 5.13 that the CDFP body is actually 60 mm x 30 mm x 16 mm, then this first model account for less than 1 % of the actual CDFP body. In addition, the driver dies, which also emit power of about 1 W each, are not included in this model.

In order to improve accuracy, at least half of the CDFP body should be modeled (recall both Tx and Rx PCB reside within the body). To encompass the large dimension, the equivalent thermal model is used to simplify complicated but repetitive geometries into a simple unit cell [80]. For example, the equivalent cell of a thermal via in glass is derived in Figure 5.23. The procedure in finding the equivalent cell is as follows:



**Figure 5.23. Simplification of a thermal via unit cell by an equivalent cell**

- 1) The unit cell is defined with a 50  $\mu\text{m}$  thick buffer layer added on either side, with 500 W/m.K conductivity. The buffer layer smooths the heat flow.
- 2) Boundary conditions is applied:  $Q''_{\text{in}} = Q''_{\text{out}} = 108 \text{ W/m}^2$ .
- 3) Simulation is performed to compute  $\Delta T$ .
- 4) The equivalent conductivity  $k$  is computed by Fourier's Law as follows:

$$Q''_{\text{in}} = k_z \frac{T_{\text{hot}} - T_{\text{cold}}}{H}, \quad (5.3)$$

and

$$Q''_{\text{in}} = k_{xy} \frac{T_{\text{hot}} - T_{\text{cold}}}{W}, \quad (5.4)$$

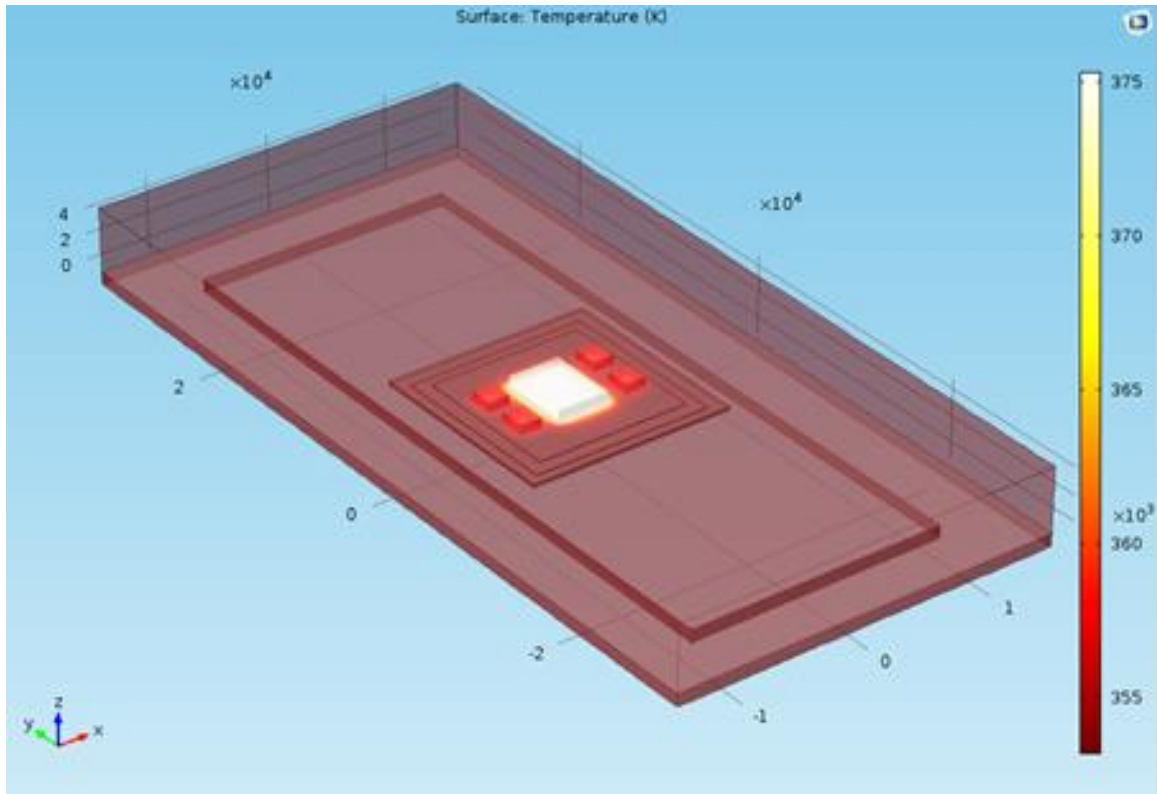
where  $H$  &  $W$  are the height and width of the unit cell, respectively. Using equivalent cell model, all circular and spherical shapes can be reduced to simple blocks, as listed in Table 5.5.

**Table 5.5. Equivalent cell model of all circular/spherical shapes in thermal model**

Unit cell	Diameter [ $\mu\text{m}$ ]	Pitch [ $\mu\text{m}$ ]	$k_z$ [W/m.K]	Notes
FLI Solder Ball	184	254	15.6*	in NAMICS underfill
TPV (Cu-Conformal)	75/5	250	1.46	5 $\mu\text{m}$ plated by SAP
SLI Solder Ball	250	500	8.4	in air, between interposer and PCB
PTH Cu-Conformal	254/127	800	18.4	in PCB

To maintain  $< 80^\circ\text{C}$  operating temperature on the PIC, it was found that  $k_z$  should be  $> 10$  W/m.K. From the table above, the bottleneck to heat dissipation is the conformal plated thermal vias with 5  $\mu\text{m}$  copper thickness. Unless the vias are filled with a thermally conductive material or plated more, they are going to be barely superior to glass in conductivity. In fact, 3D EM simulation

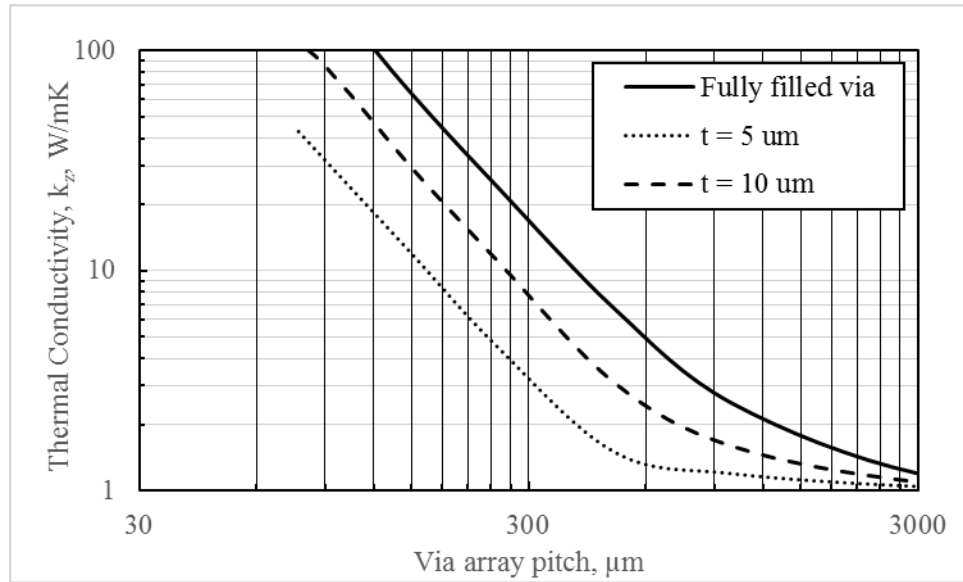
of SMTV using above equivalent model, in Figure 5.24, showed heat concentration in PIC-Tx with very little dissipation to the board.



**Figure 5.24. 3D EM simulation of the Tx module using the equivalent model, showing bottleneck to thermal dissipation at glass interface**

A parametric study of the thermal conductivity of thermal vias, in terms of pitch and copper thickness is shown in Figure 5.25. For conformal plated via with 5  $\mu\text{m}$  thickness to be effective, the via pitch will need to be 150  $\mu\text{m}$ . If the plated copper thickness along via sidewall can be increased to 10  $\mu\text{m}$ , then 250  $\mu\text{m}$  pitch is sufficient. Fortunately, even the 150  $\mu\text{m}$  pitch via array can be effectively plated in a pumped electrolytic bath. Therefore, the thermal via design is compatible with electrical processing.





**Figure 5.25. Parametric study of equivalent thermal conductivity of three different types of thermal vias at different pitch**

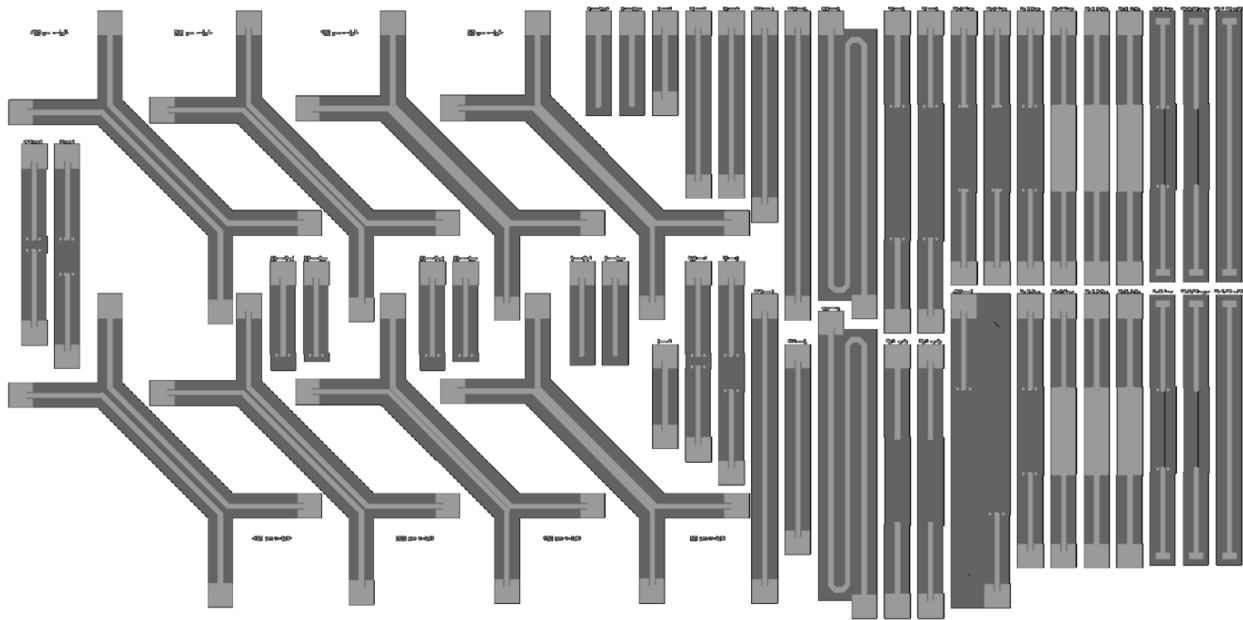
### 5.2.5 Design of Single-Mode Test Vehicle

Once modeling is completed, the design rules are fed back to design a fully integrated test vehicle in a glass panel. The ideal size of the glass panel is limited by tool capabilities. The limiting tool in GT PRC is the Ushio exposure tool, which has an exposure range for a 4 inch wafer; therefore, the ideal size of the glass panel is 4 inches, of 100 mm x 100 mm. In addition, in order to maintain consistent electroplating thickness, a 12.5 mm border around the edge of the glass panel is designated as keep-out region. Therefore, the working area within the glass panel is only 75 mm x 75 mm.

### Electrical Characterization Region

For optimum calibration of high speed electrical characteristics, a TRL kit is designed directly on the glass substrate, separated from the test vehicles, to allow in-situ calibration and de-

embedding of parasitic effects and process related variations. TRL stands for Through-Reflect-Line and it corrects the phase and magnitude errors introduced by cables, fixtures, and connectors. It works by using a through line, a reflect line either as an open or as a short, and a series of delay lines. More information regarding TRL can be found in [81]. The design and characterization of TRL kit is in collaboration with Ciena Corporation, who help designed the high speed launch pad and recommended the length of the structures to design. In addition to the TRL kit, several via transition structures, as well as crosstalk structures, are also included. These designs take up half of the glass panel working area, as shown in Figure 5.26. Table 5.6 contains a full list of the 26 electrical structures in this “electrical characterization region.”



**Figure 5.26. The electrical characterization portion of the glass panel, containing TRL structures in the middle, the cross-talk structures in the left side, and via transition structures in the right side. The dimension of the structures above is 75 mm x 37.5 mm**

**Table 5.6. Complete list of test structures on electrical characterization portion of the glass panel. All MSL pair below are 100  $\mu\text{m}$  traces with 50  $\mu\text{m}$  spacing**

Structure name	Qty.	ID	Description
Short 1	2	R1	Shorted MSL pair, 5 mm long
Short v1	2	Rv1	Shorted MSL pair, 5.3 mm long, 1 via transition
Open 1	2	R2	Open MSL pair, 5 mm long
Open v2	2	Rv2	Open MSL pair, 5.3 mm long, 1 via transition
Through 1	2	T1	Through MSL pair, 5 mm long
Through 2	2	T2	Through MSL pair, 10 mm long
Through v1	2	Tv1	Through MSL pair, 10.6 mm long, 2 via transitions
Line 1	2	L1	Delay MSL pair, 11.4 mm long
Line 2	2	L2	Delay MSL pair, 17.3 mm long
Line 3	2	L3	Delay MSL pair, 48.6 mm long
Line v1	2	Lv1	Delay MSL pair, 12 mm long, 2 via transitions
Line v2	2	Lv2	Delay MSL pair, 17.9 mm long, 2 via transitions
Line v3	1	Lv3	Delay MSL pair, 49.2 mm long, 2 via transitions
Cross 1	2	X1	2 MSL pairs, 10 mm cross-talk @ 50 $\mu\text{m}$ space
Cross 2	2	X2	2 MSL pairs, 10 mm cross-talk @ 100 $\mu\text{m}$ space
Cross 3	2	X3	2 MSL pairs, 10 mm cross-talk @ 200 $\mu\text{m}$ space
Cross 4	2	X4	2 MSL pairs, 10 mm cross-talk @ 400 $\mu\text{m}$ space
Via 1	2	V1	MSL pair, 15 mm long, 2 via transitions, no ground via next to via transition
Via 2	2	V2	MSL pair, 15 mm long, 2 via transitions, ground via 150 $\mu\text{m}$ from via transition
Via 3	2	V3	MSL pair, 15 mm long, 2 via transitions, ground via 300 $\mu\text{m}$ from via transition

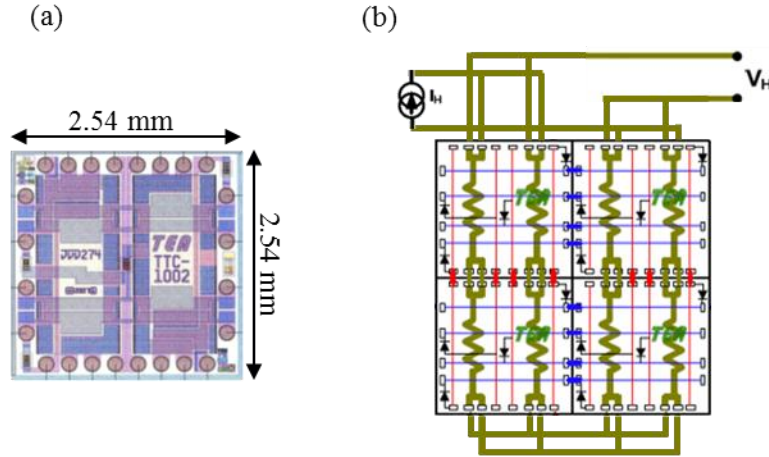
Via 4	2	V4	MSL pair, 15 mm long, 2 via transitions, 1 via each at via transition, with ground plane on top
Via 5	2	V5	MSL pair, 15 mm long, 2 via transitions, two vias at via transition, with ground plane on top
Via 6	2	V6	MSL pair, 15 mm long, 2 via transitions, four vias at via transition, with ground plane on top
Single 1	2	S1	Single MSL, 240 $\mu\text{m}$ wide, 15 mm long
Single 2	2	S2	Single MSL, 240 $\mu\text{m}$ wide, 15 mm long, 2 via transitions, no ground vias
Single 3	2	S3	Single MSL, 240 $\mu\text{m}$ wide, 15 mm long, 2 via transitions, with ground vias

### Glass Interposer Region

A 2 x 4 array of glass interposer is implemented in the remaining half of the working area of glass panel. Per recommendation from DISCO Corporation, a 0.5 mm dicing street is added.

Although Ciena provided the BOM, these dies were never procured. Fortunately, active dies are not a part of the design requirements, except for the power output for the thermal requirement. Fortunately, a thermal test chip (TTC-1002), shown in Figure 5.27, can be used to emulate the power output of PIC-Tx [82]. Each unit cell of TTC-1002 consists of two large resistors, each with a nominal resistance of 7.6  $\Omega$ . The configuration below connects the resistors in a 2 x 4 grid with total resistance of 15.2  $\Omega$ . To dissipate 6.7W of power using the configuration as shown in the figure below, simply bias  $V_H = \sqrt{(15.2 \times 6.7)} = 10.1$  V, provided that the supply can source  $I_H = \sqrt{(6.7/15.2)} = 0.66$  A.

To test the effect of thermal vias, via array of varying density is implemented in each column, with pitch of 250  $\mu\text{m}$ , 500  $\mu\text{m}$ , 1000  $\mu\text{m}$ , and infinite (no via).



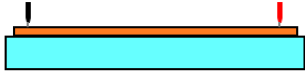
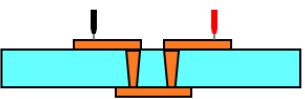

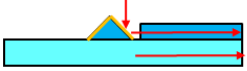
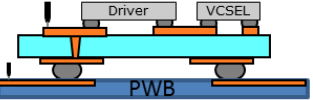
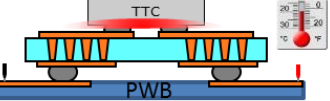
**Figure 5.27. (a) Layout view of a unit cell of TCC-1002 and (b) TCC-1002 in a 2x2 array, with the resistors connected in 2 x 4 grid**

Four MSL pairs are implemented on the interposer, with transition down to PCB, to emulate the signals coming out of the TIA to the module card. In addition, nine process monitors are placed around the interposer to monitor the quality of via formation and BGA connection, respectively.

Optically, all of the test structures described in Figure 4.15 have been transferred over to this test vehicle. In addition, the die level reliability structures from TE collaboration have been transferred over. Since the optical domain is single-mode and the TE dies are designed for multimode, there's no reason to perform electro-optical testing on these devices.

The list of all test structures on the glass panel is shown in Table 5.7.




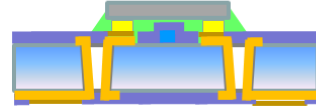







**Table 5.7. Summay of all test structures in test vehicle**

Type	Illustration	Layers	Description	#
1		M1 Only	TRL, cross-talk	12
2		M1-M2	Yield, high speed MSL & Diff	17
3		M1-PWB	High speed, board level & rel	10
4		Optical & M1	Optical coupling loss	5
5		M1 - PWB	Reliability structures, testable at board level	6
6		M1 - PWB	Thermal test chip + thermal TPV	4

### 5.2.6 Fabrication of Test Vehicle

The process flow for the second generation single-mode test vehicle (SMTV2) is shown in Figure 5.28. The first generation single-mode test vehicle uses TIR turning design, which includes a lens reflow process. Only results from SMTV2 will be shown here.

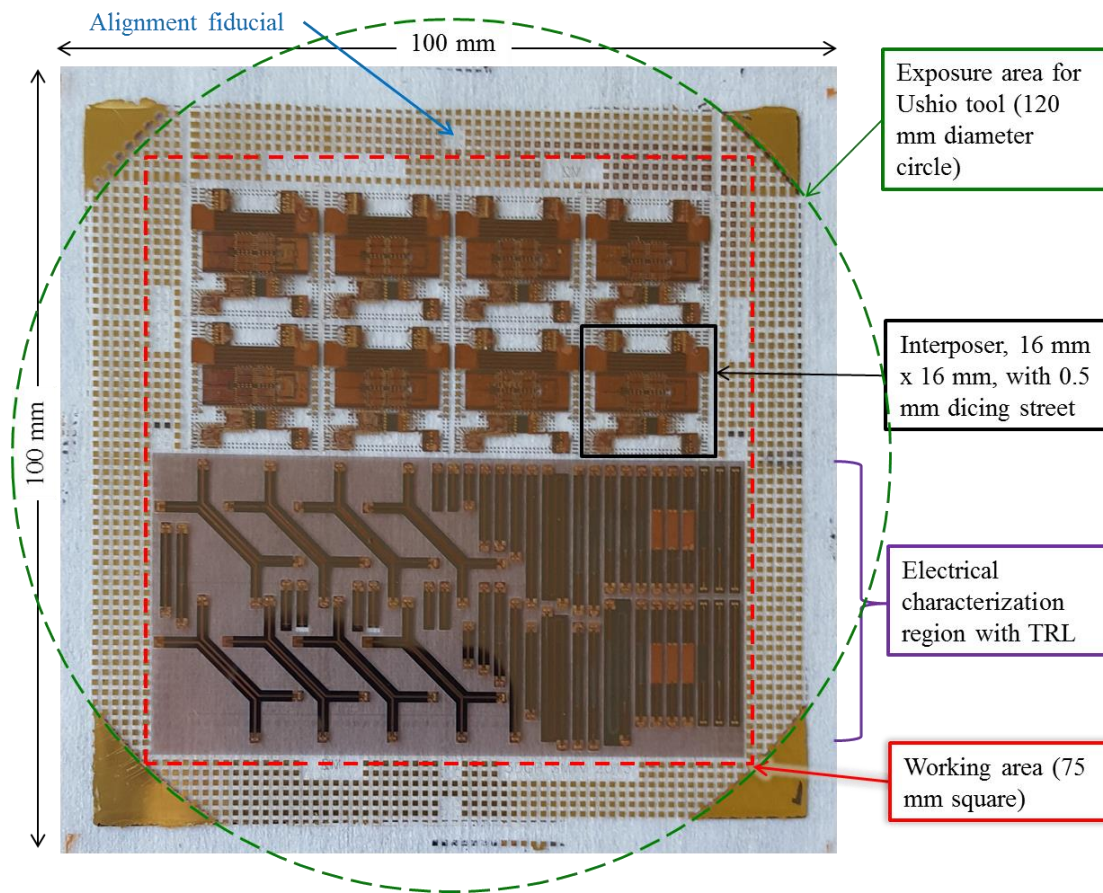
Since all of the process steps have been described in detail in section 5.3, overlapping process steps will not be repeated here. The only difference is the addition of Bondfilm process, a wet process provided by Atotech performed on electroplated copper prior to application of dry film BCB passivation layer. The top view of a completed panel prior to ENIG is shown in Figure 5.29.

Figure	Process Step	Figure	Process Step
	TGV formation		ENIG surface finish
	Copper seed layer		Die assembly by reflow
	SAP		BGA balling
			Singulation
	Optical layer		Board Assembly & Fiber Attach
	Solder Resist / Cladding		

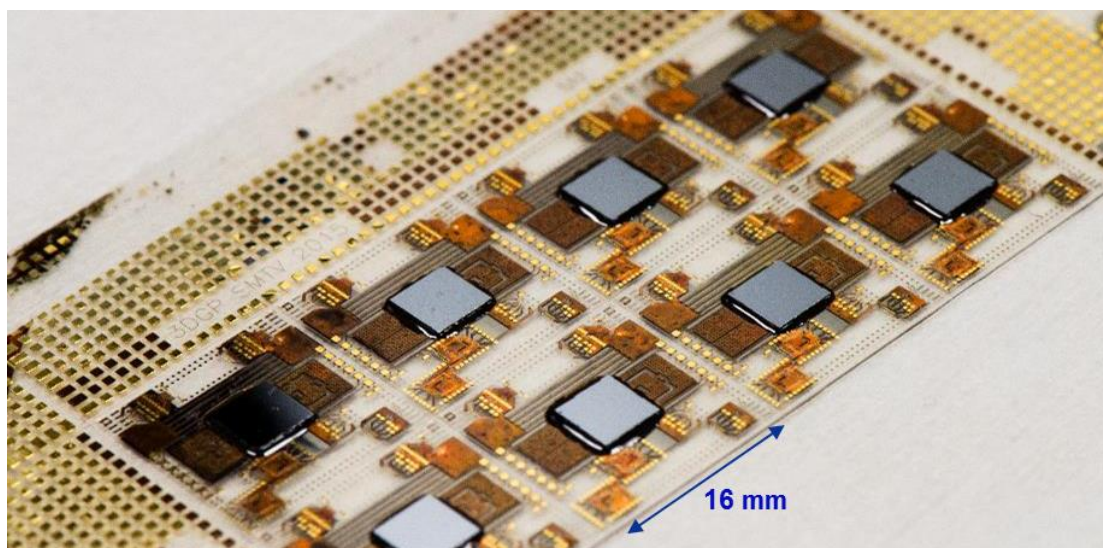
**Figure 5.28. Process flow for Single-Mode Test Vehicle, part 2 (SMTV2)**

The electrical characterization region does not need ENIG treatment because the electroless plated nickel can act as a parasitic at high frequencies; in fact, the bottom half of the panel is removed prior to ENIG.

Yield is assessed across 10 panels prior to assembly by measuring the resistance across a daisy chain structure of vias within each interposer. Of the 80 interposers tested, 76 passed equating to 95% yield. The thermal test chips are assembled after yield test. The assembled panel is shown in Figure 5.30. After the dies are assembled, BGAs are printed on the back side and reflowed, as shown in Figure 5.31.

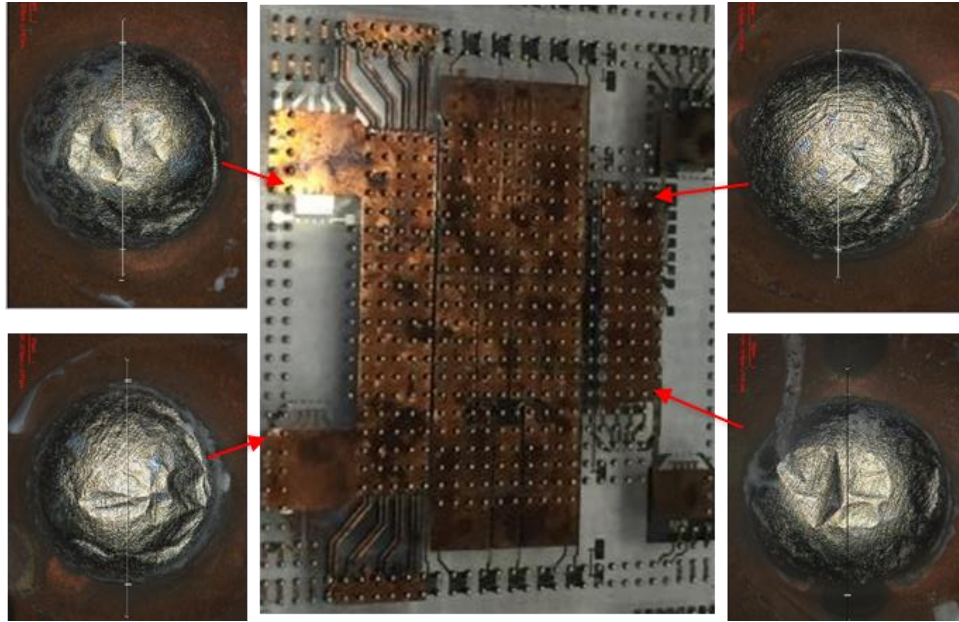


**Figure 5.29. Top view of a SMTV2 glass panel prior to ENIG process**



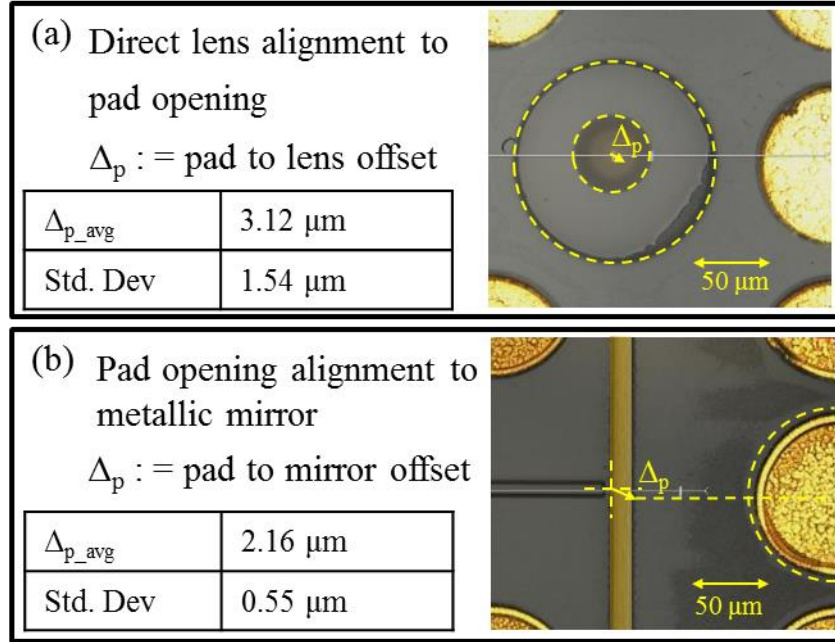
**Figure 5.30. The top half of glass panel after ENIG and chip assembly**





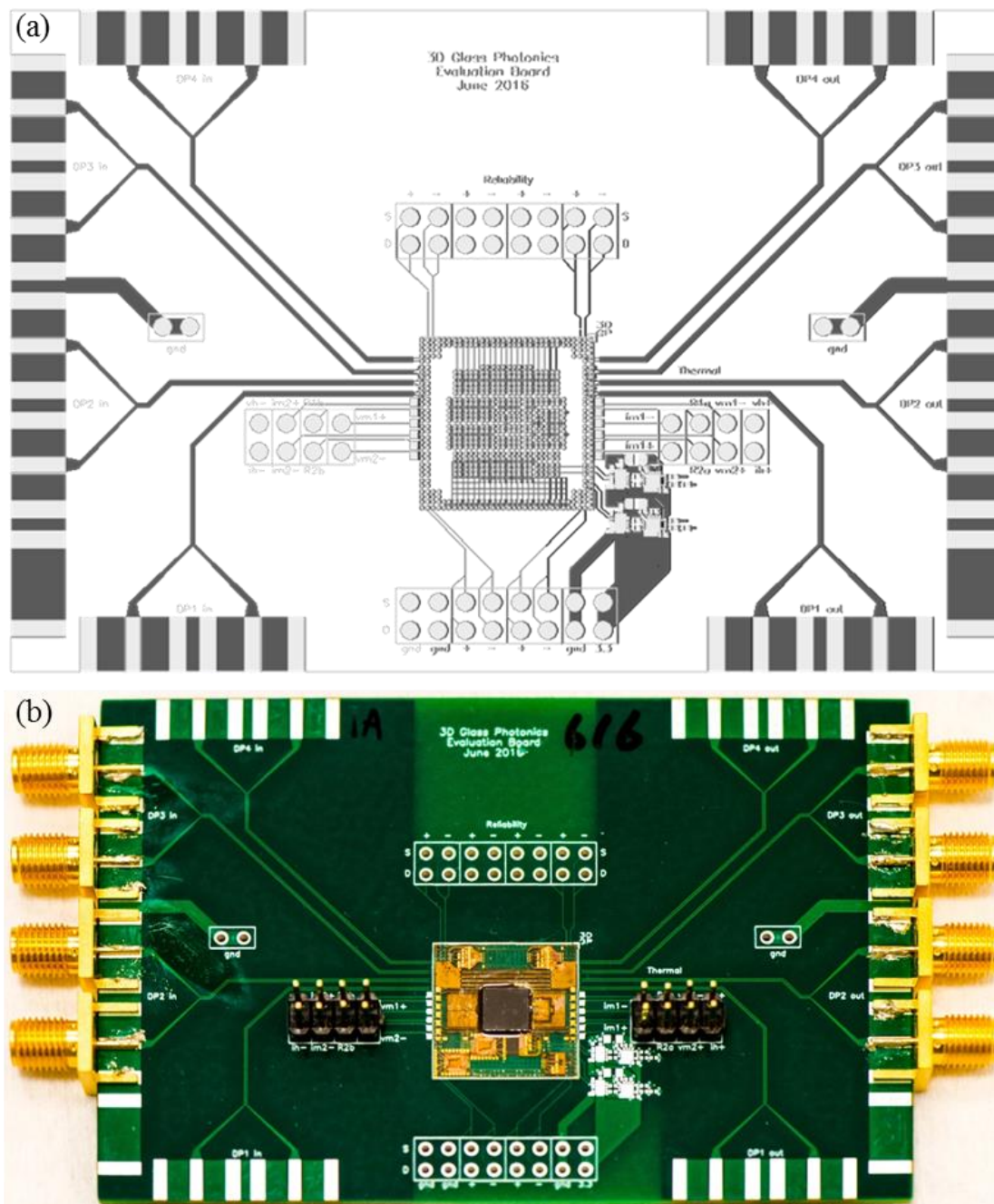
**Figure 5.31. Reflowed BGA balls on the backside of interposer. The height variation of the BGA balls is  $5\text{ }\mu\text{m}$  across panel, equating less than  $3\text{ }\mu\text{m}$  variation across interposer, less than 2 % of the stand-off height of second level interconnect**

Of critical importance is the fabrication alignment tolerance between the electrical pads and the optical coupling structures. Recall, from Chapter 4, the 1-dB alignment tolerance between chip and the turning mirror or the plano-convex lens is between 2 to  $2.5\text{ }\mu\text{m}$ . The fabrication tolerance is studied across the panel, and the results are shown in Figure 5.32. Direct alignment is possible in both cases – for the TIR turning the lens is directly aligned to the pad opening, whereas for the metallic turning the pad opening is directly aligned to the turning mirror. While the misalignment is great than  $2\text{ }\mu\text{m}$  across the panel, it is likely due to the warpage of the glass panel across the panel and can be controlled better with a dedicated frame using fabrication.



**Figure 5.32. Fabrication tolerance study for the alignment of out-of-plane turning structures to gold pads for chip assembly**

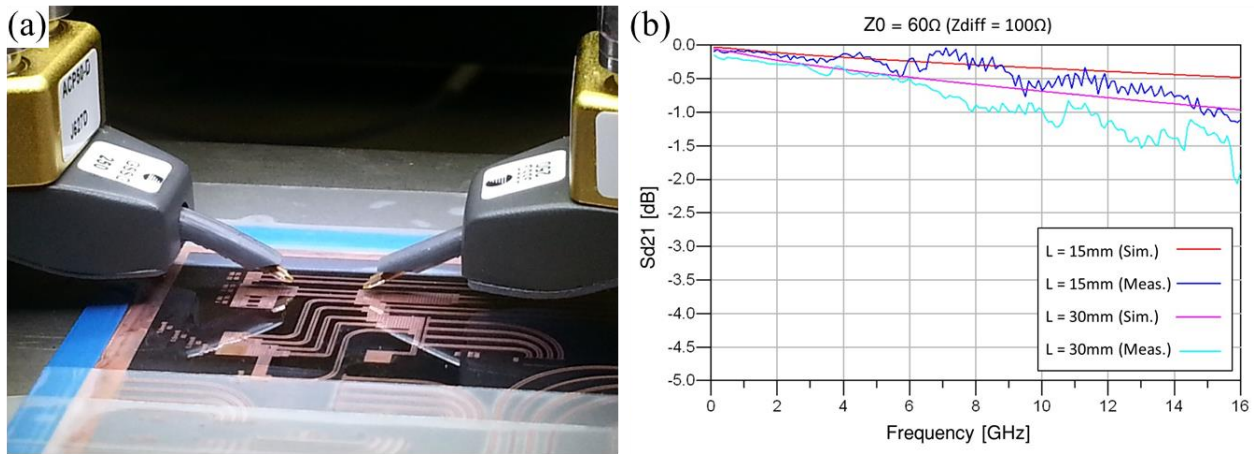
The custom designed PCB has been contracted out by PCB Universe, it is shown in Figure 5.33. Eight SMTV coupons, diced by DISCO Inc., have been assembled on the PCBs to allow for electrical and thermal testing, also shown in the figure. Electrical connectivity tests have been performed on the coupons, with six points taken from each coupon. The yield is 83% (40/48), where four is attributed to dicing as delamination can be observed along the diced edge, two is attributed to the plating of TGVs from electrical testing, and two is attributed to missing or deformed BGAs by visual inspection.



**Figure 5.33. (a) Layout and (b) assembled PCB with SMTV interposer in lower center. The dimension is 60 mm x 90 mm**

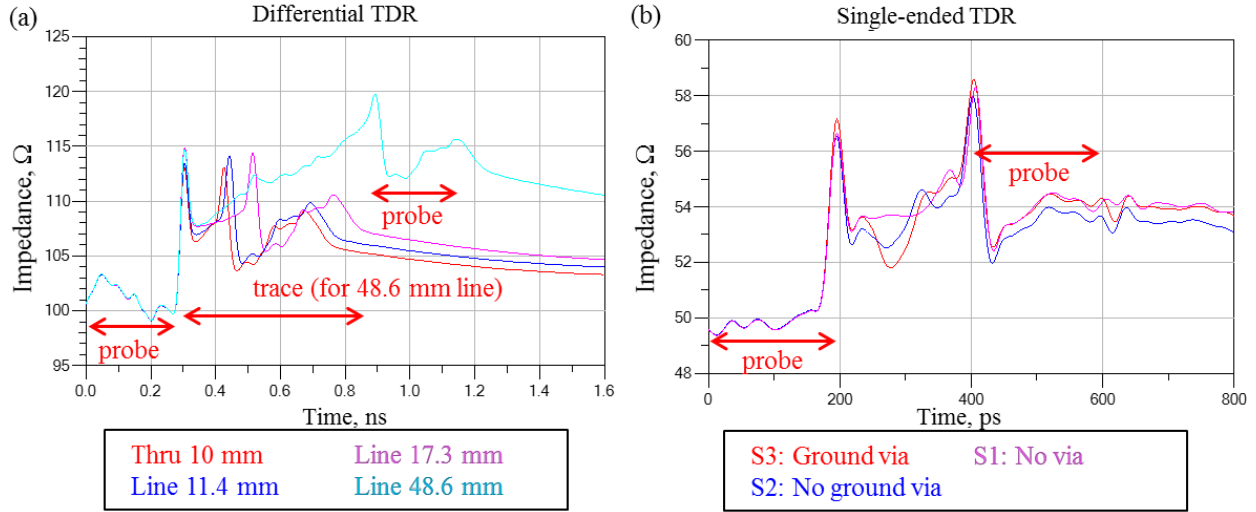
### 5.2.7 Characterization of Test Vehicle

Only optical and electrical characterization data have been collected at this point. The  $S_{21}$  of the differential MSL have been measured in house using a Vector Network Analyzer, as shown in Figure 5.34. While the measured  $S_{21}$  is noisier comparing to simulation, the loss remains quite low at less than 0.1 dB/mm rate, an order of magnitude lower than the design requirement.

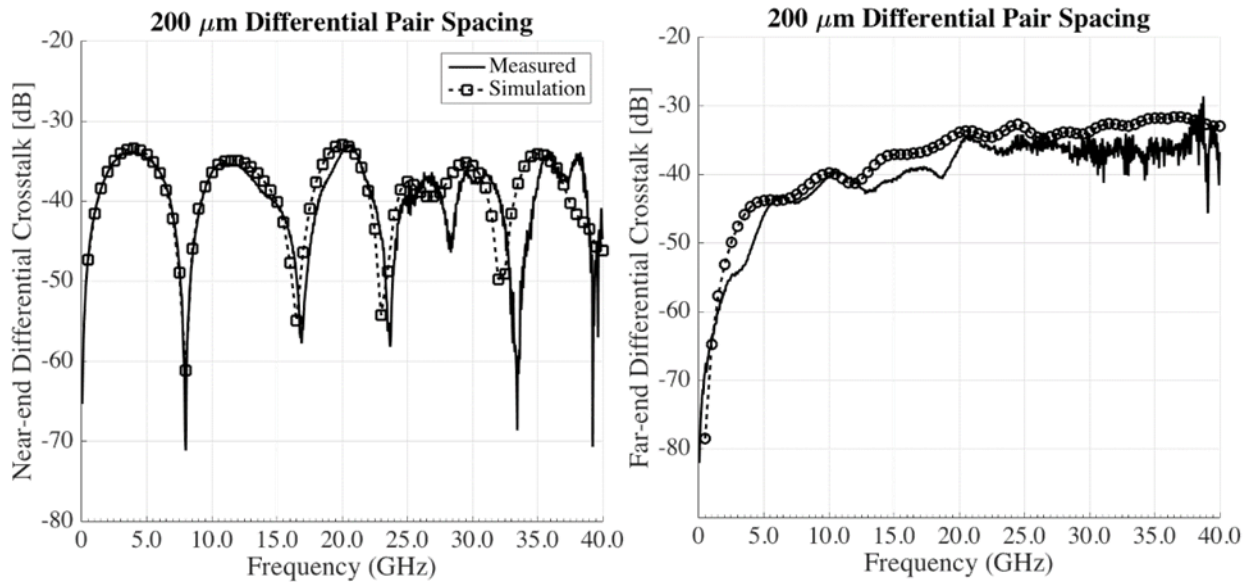


**Figure 5.34. (a) VNA setup for electrical characterization and (b) measured  $S_{21}$  as compared to simulation**

The impedance of the traces is measured by TDR (Time Domain Reflectometry) method for both single ended and differential signals, as shown in Figure 5.35. The measured impedance is 105 and 53, respectively. The consistently higher measurement can be attributed to the glass thickness being thinner than anticipated. The crosstalk structures are measured by Ciena in their facility in Ottawa because the number of ports required (four differential) exceeded the capability at GT PRC. The closest spacing for which the crosstalk is below 30 dB is 200  $\mu\text{m}$ , as shown in Figure 5.36. The measured data matches closely with simulation up to 40 GHz.



**Figure 5.35. TDR measurement of (a) differential MSL and (b) single-ended MSL**



**Figure 5.36. Measured versus simulated differential crosstalk at 200  $\mu\text{m}$  spacing for (a) near-end and (b) far-end**

The optical data have already been presented in Chapter 4. At the writing of this thesis the thermal characterization is still not ready.

### 5.3 Summary

The main objective of design and demonstration test vehicles has been to integrate the fundamental research building blocks in a realistic package design. Two such photonics test vehicles have been presented in this chapter – the reliability test vehicle (RTV) with 2.5 D integration of VCSEL and driver dies, and the single-mode test vehicle (SMTV, SMTV2) with co-design of optical, electrical, and thermal interconnects.

The reliability test vehicle (RTV) was a collaboration with TE Connectivity, who provided both the active devices as well as the reference design. The main objective of RTV was to study the reliability of 2.5 D photonics integration on glass interposer, by warpage analysis and thermal cycling test. The challenges were to limit the warpage of interposer by careful design of stack-up, and to develop a process to assembly VCSEL dies using AuSn solder at 280 °C eutectic and Driver dies using SnAg solder at 250 °C reflow. A customized glass substrate build-up process flow based on direct metallization was developed to minimize interposer warpage to less than 10  $\mu\text{m}$ . On the other hand, a sequential assembly flow was developed to reflow VCSEL dies, then reflow driver dies, on a glass interposer. Electrical testing before and after reliability testing showed no failure. Energy Dispersive Spectroscopy (EDS) scan of cross-sectioned interconnections revealed hairline cracks formed not from reliability testing, but at time zero due to bump damage and pad shape non-coplanarity. Although not a failure, the cracks can be minimized by changes to pad design if needed. The reliability study concluded successfully.

The single-mode test vehicle (SMTV & SMTV 2) was a multi-year collaboration between GT-PRC, TE Connectivity, and Ciena Corporation, who provided device specs for modeling and floor planning. The main objective of SMTV was to emulate the 400 Gbps Form-factor Pluggable (CDFP) optical transceiver by combining the out-of-plane single-mode optical interconnections



presented in Chapter 4 with high speed electrical and thermal interconnects. Design requirements in each physics was defined based on device specifications and literature research. A co-design process was developed to ensure all design requirements were met while maintaining non-interfering signal and power flow, and that a compatible process could be developed. Once the co-design had been completed the test vehicle was fabricated using a similar process as the RTV, except with an added optical process step as described in Chapter 4. Process monitor test showed 95% yield, and the metallic turning structure was shown to meet the fabrication tolerance requirement of 2.5  $\mu\text{m}$ . High speed electrical testing showed propagation loss an order of magnitude lower than design requirement at 14 GHz, highlighting the advantage of glass substrate for high speed electrical. The microstrip line spacing that ensures less than 30 dB of crosstalk was found to be 200  $\mu\text{m}$ , consistent with package level cross-talk spacing.

In summary, the design and demonstration test vehicles offered an opportunity to integrate fundamental research components to emulate an actual system-on-package. In RTV and SMTV, optical, electrical, and thermal interconnect were combined with 2.5 D chip assembly. The results showcased the capability of GT-PRC in executing multidisciplinary research and development.

## CHAPTER 6

### CONCLUSIONS

This dissertation presented some of the first research results on glass substrates with 3D photonics interconnections to address the critical need for highest bandwidth at lowest power consumption and cost for board-board optical communication. In contrast to the prior research on silicon photonics and board-level optoelectronics, the 3D glass photonics interposer technology achieves higher density in both optical and electrical domains, utilizes large panel processing for cost reduction, and uses 3D optoelectronics packaging for ultra-low loss interconnections. This chapter summarizes the research results, presents the significant technical contributions from this research, and identifies future research directions in glass photonics.

The main objective of this research was to design and demonstrate 3D glass photonics interconnections. The specific focus of this dissertation research was to design and demonstrate low loss and high tolerance out-of-plane single-mode fiber-to-chip optical interconnections in ultra-thin glass interposers. Three specific technical challenges were identified to achieve these objectives as follows: 1) low loss optical interconnections in glass to address the challenge in high fiber-to-chip coupling loss, 2) scalable out-of-plane turning structures to address the lack of high density fiber-to-chip coupling solutions, and 3) design for high tolerance fiber alignment to address the costly active fiber alignment. Four research tasks were defined, one task each to address each challenge, and a fourth task focused on a demonstration test vehicle.

#### 6.1 Summary of Results

The four research tasks, their targets, and the results achieved in this thesis, are summarized in Table 6.1. The first three tasks involved in-depth investigation of fundamental building blocks of



the out-of-plane fiber-to-chip optical interconnections including the optical waveguide, the turning structure, and the fiber alignment groove. In task four, these optical interconnections are integrated with electrical and thermal building blocks at package level, with 2.5 D active device assembly, to emulate an optical transceiver module.

**Table 6.1. Summary of research tasks, targets, and results**

Research Tasks	Targets	Results
Low loss and high tolerance large core single-mode optical waveguides or vias in glass	< 1 dB fiber-to-WG coupling loss	0.38 dB simulated 0.9 dB measured
	< 1 dB/cm WG loss	< 1 dB/cm via measured <b>&gt; 1 dB/cm WG measured</b>
	1-dB x & y tolerance 1-dB angle tolerance	$\pm 2 \mu\text{m}$ & $\pm 2^\circ$ simulated
Out-of-plane turning mirror using moving mask lithography	< 2 dB chip-to-fiber coupling loss	0.82 dB simulated 1.69 dB measured
	Turning angle tolerance	1.5° simulated 1° achieved
	WG to turning mirror alignment tolerance	3 $\mu\text{m}$ simulated 1.6 $\mu\text{m}$ achieved
	High throughput	4" panel process
Optical fiber alignment grooves in glass	Meets 1-dB x & y tolerance	$\Delta_x < 2 \mu\text{m}$ <b><math>\Delta_y &gt; 2 \mu\text{m}</math></b>
	Meets 1-dB z tolerance	<b><math>\Delta_z &gt; 50 \mu\text{m}</math></b>
Design and demonstration test vehicle	2.5 D assembly of VCSEL & Driver	Reliability testing passed

	Optical to electrical alignment	2.5 $\mu\text{m}$ simulated 2.16 $\mu\text{m}$ achieved
	25 Gbps electrical	Design requirement passed, measurement confirmed
	Thermal via	Design requirement passed

### 6.1.1 Low Loss Single-Mode Optical Waveguides and Vias

Single-mode optical waveguides both planar to the surface of glass and traveling through glass have been studied by Gaussian beam analysis, finite element simulation, fabrication process optimization, and optical characterization.

Planar waveguides are fabricated using a polymer core, polymer upper cladding, and glass substrate as under cladding. The low refractive index difference between the core and upper cladding enables a large waveguide core for single-mode propagation as proven by effective refractive index simulation. This large core waveguide has shown fiber coupling loss less than 1 dB both in simulation and measurement. Cutback optical loss measurement of the waveguide is in excess of 1 dB/cm, which may be a combination of material property and surface defects.

Optical vias and lens waveguides are investigated for vertical transmission. Optical vias provide optical confinement by total internal reflection irrespective to glass thickness; however, optical via fabrication is challenging and costly. Lens waveguides can achieve 100 % coupling efficiency; however, micron-level variation in lens dimension will cause the efficiency to drop off. Bare glass transmission is sufficient for thin glass up to 30  $\mu\text{m}$  thickness, beyond which optical vias are useful if they can be fabricated. Optical measurement of fabricated multimode vias has shown < 1 dB/cm propagation loss.

The 1-dB alignment tolerance of vias and waveguides have been studied by Beam Propagation Modeling. The large core design in glass contributed to excellent tolerance of  $\pm 2 \mu\text{m}$  in x & y direction,  $\pm 2^\circ$  in  $\theta_x$  and  $\theta_y$ , and  $> 50 \mu\text{m}$  in z.

### **6.1.2 Out-of-Plane Turning Structures**

Moving mask lithography can achieve high throughput and consistency by moving the entire mask during exposure, thus enabling turning structures to be made throughout the entire panel using wafer-level technologies such as spin coating and puddle development. Tailorable turning angle can be achieved by adjusting the shutter opening time and movement distance of the stage. Using moving mask lithography, turning mirrors at both  $41^\circ$  and  $45^\circ$  have been realized within  $1^\circ$  across a glass panel.

Two different out-of-plane turning structures have been studied: Total-internal-reflection (TIR) turning and metallic turning. Metallic turning structure is superior both in terms of coupling efficiency, fabrication tolerance, alignment tolerance, and long term reliability. Optical simulation of the metallic turning structure coupling to a vertical grating coupler (VGC) shows coupling loss of only 0.82 dB excluding the loss from VGC itself, much less than the 2 dB target. Optical measurement of the metallic turning structure shows turning loss less than 1.69 dB, still within the target. The tolerance required to achieve 1-dB loss is  $\pm 3 \mu\text{m}$  for the waveguide to turning mirror alignment and  $\pm 1.5^\circ$  for the turning angle, both of which have been met in fabrication.

### **6.1.3 Fiber Coupling Grooves**

Unlike crystalline silicon, precision micro-structuring in amorphous glass has been challenging. Two different fiber alignment groove structures using mechanical dicing have been explored: two-point contact u-groove and shallow cut u-groove. While the two-point contact u-groove was able

to achieve  $\Delta_x$  requirement, it failed in  $\Delta_y$  direction. The shallow cut u-groove was able to address the  $\Delta_y$  alignment, but could not meet  $\Delta_z$ . Further research efforts are needed beyond the scope of this thesis to develop a solution to fiber coupling to glass.

#### **6.1.4 Design and Demonstration Test Vehicles**

Two design and demonstration test vehicles have been presented – the reliability test vehicle (RTV) with 2.5 D integration of VCSEL and driver dies, and the single-mode test vehicle (SMTV, SMTV2) with co-design of optical, electrical, and thermal interconnects.

The reliability test vehicle (RTV) was a collaboration with TE Connectivity. The main objective of RTV was to study the reliability of 2.5 D assembly of a VCSEL die and a driver die on glass interposer by thermal cycling test. The challenges were to limit the warpage of interposer and to develop a process to assembly VCSEL dies using AuSn solder and Driver dies using SnAg solder. Interposer warpage of less than 10  $\mu\text{m}$  was achieved by direct metallization of copper on glass substrate, with a symmetric build-up. A sequential process was developed to assemble VCSEL dies then driver dies on glass. Electrical testing before and after reliability testing showed no failure. Energy Dispersive Spectroscopy (EDS) scan of cross-sectioned interconnections revealed only hairline cracks due to bump damage and pad shape non-coplanarity. Therefore, the reliability results were successful.

The single-mode test vehicle (SMTV & SMTV 2) was a collaboration with TE Connectivity and Ciena Corporation. The main objective of SMTV was to emulate the 400 Gbps Form-factor Pluggable (CDFP) optical transceiver by combining low loss optical, high speed electrical, and thermal interconnections in glass. A co-design strategy was developed to ensure design requirements were met without interfering with each other, and that a compatible process could be developed. The test vehicle was fabricated using a novel process flow aligning the electrical and

optical circuitry to through glass vias. 95% yield was observed after fabrication. The metallic turning structure alignment to gold pads was measured 2.16  $\mu\text{m}$ , within the fabrication tolerance requirement of 2.5  $\mu\text{m}$ . High speed electrical testing showed propagation loss of  $< 0.1$  dB/mm, an order of magnitude lower than design requirement at 14 GHz. While modeling showed conformal plated thermal vias to be an ineffective way to dissipate heat, a dense via array at 250  $\mu\text{m}$  pitch or below could still meet the 80 °C target.

## **6.2 Technical and Scientific Contributions**

The key contributions from this thesis are as follows:

1. Developed the first “glass photonics” technology utilizing thin glass panels and high volume substrate processes.
  - a. Co-design of optical, electrical, and thermal requirements.
  - b. Process flow to allow high yield fabrication of optical and electrical interconnections.
  - c. Reliability qualification featuring 2.5 D assembly of active devices.
2. In-depth analysis of single-mode out-of-plane chip-to-fiber optical interconnections in glass to address the high cost of packaging in optical communication systems.
3. Demonstration of novel polymer optical vias in glass and defined application space for such vias as superior means for vertical transmission through glass.
4. Development of novel moving mask lithography to fabricate low loss and high tolerance turning mirror in glass.

### **6.3 Recommendation for Future Work**

While key contributions have been made, many more opportunities for future development have been identified during the course of this thesis. It has been a true testament that advancements in scientific knowledge are built on countless failures and trials, and that there will always be more room for exploration and improvement. Three key areas for future works have been identified.

#### **6.3.1 Fiber Coupling by Pick-and-Place in Glass Cavities**

One of the key learnings from the research work concerning u-grooves had been the need to establish z-direction reference between optical fibers and waveguides. The diced grooves were unable to achieve this due to the radius of curvature of the dicing saw. Recently, precise glass cavities have been demonstrated by Schott glass and GT-PRC, thus opening up a possibility to establish y and z reference passively by glass cavities. The establishment of x-direction reference can be done lithographically, in the same layer as the waveguide core, thus maximizing alignment between waveguide core and fiber core, with only fiber diameter and core concentricity as variables. In addition, a pick-and-place assembly process is being developed in GT-PRC utilizing a v-groove shaped tool head to ensure fibers can be placed in the cavity with minimum angular shift.

#### **6.3.2 Circular Waveguides on Glass**

Although the waveguide core is already quite large thanks to the small refractive index difference between the core and the upper cladding, it can be even larger if the waveguide shape can be made circular, rather than trapezoidal. Fortunately, the waveguide core and cladding materials' natural tendency to reflow can be used to create truly circular waveguides without sharp corners that introduces diffraction. Close collaboration with the material supplier, Dow Chemical,

is underway to develop an under-cladding layer with a circular groove for the core to sit in. If the circular waveguide can be fabricated, it promises to have less than 0.1 dB coupling loss to an optical fiber and close to  $\pm 2.5 \mu\text{m}$  alignment tolerance.

### **6.3.3 System-Level Optimization of Glass Photonics and Silicon Photonics**

It is the opinion of the author that glass photonics and silicon photonics are not competing technologies. Rather, glass photonics is positioned to be the ideal packaging technology for silicon photonics, which is best suited at smaller dimensions. Some of the larger passive optical circuitries available in silicon photonics such as array waveguide grating (AWG) and Mach-Zander Interferometer (MZI) can be built on glass with some initial effort in process development. In addition, building V-grooves on silicon photonics dies have proven to be a major challenge, as the SOI substrate contains active CMOS circuitry that must be protected from chemical etching and during fiber assembly process. Even the edge emitting lasers (EEL), currently epitaxial bonded on SOI at wafer level to provide light source to silicon photonics, can be assembled on glass using 2.5 D technology.

A system level co-design strategy based on process cost modeling should be performed to determine the most cost efficient placement of each component of an optical transceiver – whether it should reside in glass photonics interposer or silicon photonics die. In the author's opinion, the following building blocks should remain on silicon: Ring-resonator modulators, photodetectors, optical add-drop filters, and immediate electrical interface. The following should be on glass: fiber coupling interface, EEL assembly, large coupling structures such as MZI. Some components, such as the AWG, will likely be implemented on both sides depending on design requirements.

## 6.4 List of Publications and Honors

### Journal Publications

1. **B. Chou**, W. Vis, R. Furuya, V. Sundaram, R. Tummala, “Modeling, Design, Fabrication, and Characterization of Ultra-high Bandwidth and Cost Effective Glass Photonic Substrates,” *Journal of Microelectronics and Electronic Packaging (JMEP)*, Vol. 13, No. 2, pp. 51-57, April 2016
2. **B. Chou**, W. Vis, F. Liu, V. Sundaram, R. Tummala, “Low Loss and High Tolerance Through-Glass Optical Interconnections in 3D Glass Photonic (3DGP) Interposers,” submitted to *IEEE Transactions on Components, Packaging and Manufacturing Technology*, May 2016
3. **B. Chou**, B. Sawyer, W. Vis, R. Furuya, F. Liu, V. Sundaram, R. Tummala, “Co-Design and Demonstration of a Fully Integrated Optical Transceiver Package Featuring Optical, Electrical, and Thermal Interconnects in Glass Substrate,” submitted to *Journal of Microelectronics and Electronic Packaging (JMEP)*, September 2016
4. **B. Chou**, R. Furuya, B. Khan, F. Liu, V. Sundaram, R. Tummala, “Design and Demonstration of Single-Mode Out-of-Plane Optical Interconnections in Glass Substrates,” to be submitted to *IEEE Transactions on Components, Packaging and Manufacturing Technology*, October 2016
5. T. Huang, **B. Chou**, J. Tong, H. Sharma, V. Sundaram, R. Tummala, “High Reliability Electroless Copper Metallization of Via-First Glass Interposers Using a Thin, Patternable Polymer Film,” submitted to *IEEE Transactions on Components, Packaging and Manufacturing Technology*, August 2016
6. W. Vis, **B. Chou**, F. Liu, V. Sundaram, R. Tummala, “Design and Demonstration of Self-Aligned Optical Turning Structures in 3D Glass Photonic (3DGP) Interposers,” submitted to *IEEE Transactions on Components, Packaging and Manufacturing Technology*, September 2016

### Conference Publications

1. **B. Chou**, et al, “Design and Demonstration of Micro-mirrors and Lenses for Low Loss and Low Cost Single-Mode Fiber Coupling in 3D Glass Photonic Interposers,” in *IEEE Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, June 2016 (Student Travel Award)



2. B. Sawyer, **B. Chou** *et al.*, “Design and Demonstration of 2.5D Glass Interposers as a Superior Alternative to Silicon Interposers for 28 Gbps Signal Transmission,” in IEEE Electronic Components and Technology Conference, Las Vegas, NV, June 2016
3. **B. Chou**, *et al.*, “Modeling, Design, Fabrication, and Characterization of Ultra-high Bandwidth 3D Glass Photonic Substrates,” in International Symposium on Microelectronics, Vol. 2015, No. 1, pp. 603-608, 2015.
4. W. Vis, **B. Chou**, *et al.*, “Self-Aligned Chip-to-Chip Optical Interconnections for Ultra-Thin 3D Glass Interposers,” in IEEE Electronic Components and Technology Conference (ECTC), San Diego, CA, May 2015
5. T. Huang, **B. Chou** *et al.*, “Novel copper metallization schemes on ultra-thin, bare glass interposers with through-vias,” in IEEE Electronic Components and Technology Conference, San Diego, CA, May 2015
6. B. Sawyer, **B. Chou** *et al.*, “Modeling, design, and demonstration of 2.5D glass interposers for 16-channel 28 Gbps signaling applications,” in IEEE Electronic Components and Technology Conference, San Diego, CA, May 2015
7. S. Gandhi, **B. Chou** *et al.*, “Ultra-thin and ultra-small 3D double-side glass power modules with advanced inductors and capacitors,” in IEEE Electronic Components and Technology Conference, San Diego, CA, May 2015
8. **B. Chou**, *et al.*, “Modeling, Design, and Demonstration of Ultra-miniaturized and High Efficiency 3D Glass Photonic Modules,” in IEEE Electronic Components and Technology Conference (ECTC), Orlando, FL, May 2014.
9. Y. Sato, **B. Chou** *et al.*, “RF Device Integration on Glass Interposer toward 3D-IPAC Packages,” in International Symposium on Microelectronics (IMAPS), October 2013
10. Y. Sato, **B. Chou** *et al.*, “Ultra-miniaturized and surface mountable glass-based 3D IPAC packages for RF modules,” in IEEE Electronic Components and Technology Conference (ECTC), Las Vegas, NV, May 2013
11. **B. Chou** *et al.*, “Modeling, Design, and Fabrication of Ultra-high Bandwidth 3D Glass Photonics (3DGP) in Glass Interposers,” in IEEE Electronic Components and Technology Conference (ECTC), Las Vegas, NV, May 2013 (Student Travel Award)

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